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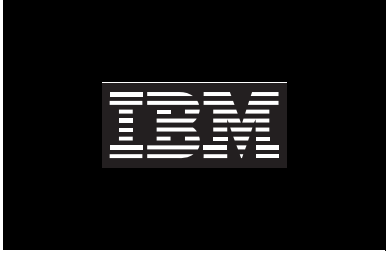


Introduction to the IBM PowerPC 476FP Embedded Processor Core

James Cuffney, Chris Harrison, Celso Furtado

Features and attributes

- *SMP enabled (scalable from 4,000 to 32,000 DMIPS)*
- *Double-precision floating-point unit exceeding three GFLOPS*
- *Coherency support for processors and I/O masters*
- *Superscalar, up to 5-issue, 9-stage pipeline*
- *Optimized multitasking, multiprocessor memory subsystem*
- *32 KB L1 caches and 256 KB - 2 MB configurable L2 cache*
- *Extensive embedded debug facilities*
- *Power Architecture V2.05E compliant (32-bit)*

Introduction

To meet the future requirements of high-performance embedded processor applications, IBM has extended its PowerPC® 4xx roadmap with the IBM® PowerPC 476FP embedded processor core. Like its predecessors, the PowerPC 476FP core provides a straightforward next step for existing customers and an enticing level of power and performance for new customers. Backward software compatibility is a key feature of this offering, and includes support for those customers who have implemented the on-board digital signal processing (DSP) instruction complement to the IBM Power Architecture® instructions.

Optimized for both single and multiple cores, the PowerPC 476FP microarchitecture meets the needs of aerospace and defense, digital televisions and set-top boxes, industrial controllers, network communications, printers and imaging products, and storage applications. These application areas, with their compute-intensive workloads, can leverage both the advanced PowerPC 476FP microarchitecture and its tightly integrated floating-point unit that exceeds three gigaflops (GFLOPS). Typically, these markets prefer processor offerings such as the PowerPC 476FP core that are designed for performance first, with a keen eye on power.

Like other PowerPC 4xx family offerings, the robust PowerPC 476FP design includes the development and support infrastructure that helps customers bring solutions to market quickly and cost effectively. A complete Linux® tool chain and GCC compiler are available today, with support for other major operating systems and integrated development environments underway.

Historically, PowerPC 4xx customers have limited their multiple-core solutions to an asymmetric multi-processor (AMP) approach, allowing them to control system resources, optimize system performance and reliability, and manage system power, all while protecting legacy code investments. Looking ahead, the need to support a wide variety of coherent masters, including coherent I/O masters, in a symmetric multi-processing (SMP) environment is clear. To that end, IBM is also introducing an extension to the CoreConnect™ architecture, the processor local bus 6 (PLB6), that is capable of providing a scalable coherency fabric for up to eight

Power and performance

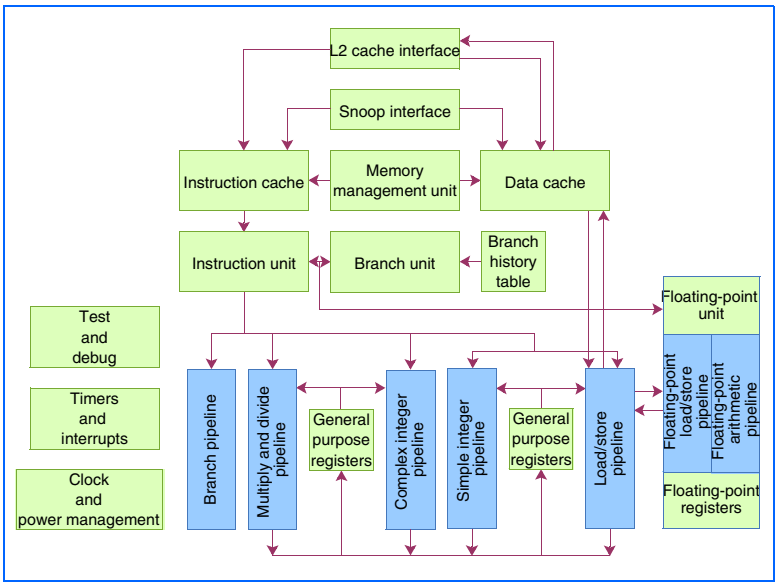
- *1.6 GHz+ operation*
- *2.5 DMIPS per MHz (Dhrystone 2.1)*
- *0.9 to 1.1 V voltage range in IBM 45 nm SOI*
- *-40 to 125°C operating temperature range*

masters. Developers can now take advantage of the benefits of either SMP or AMP to optimize their system-on-chip (SoC) architectures.

The PowerPC 476FP offering also includes the multi-processor interrupt controller (MPIC) and the level 2 cache/coherency controller. These elements, in conjunction with the PowerPC 476FP core and the PLB6, enable a level of coherent scalability that customers can use to create software-seamless families of product offerings.

The IBM PowerPC 476FP offering is the latest addition to the family of PowerPC 4xx embedded processors, designed for leading-edge SoC applications. Its protection of legacy software investments explains its rapid adoption by existing customers. Its performance and power optimization, on-board DSP instructions, tightly coupled floating-point unit, and fully coherent scalable SoC capabilities will lead to its rapid adoption by customers new to the PowerPC 4xx family of Power Architecture offerings.

The following figure shows the logical organization of the 476FP processor core.

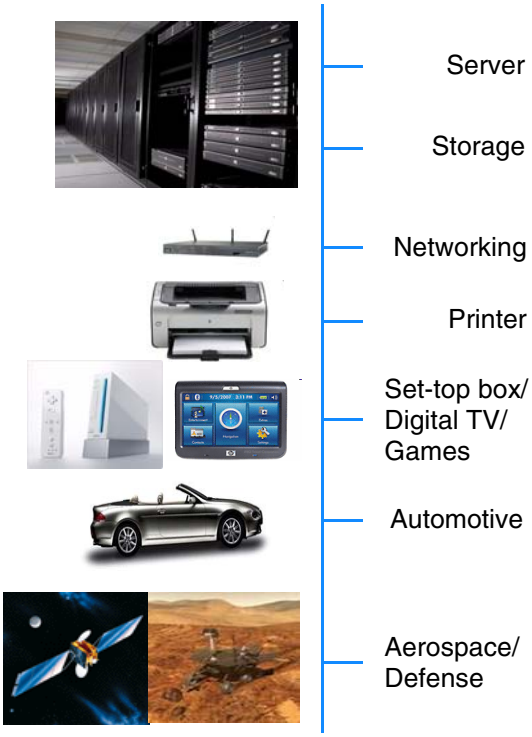


Value proposition

- *Software compatibility/investment protection*
  - *Unified ISA that spans multiple customer projects*
  - *Design flexibility for diverse specialization*
  - *IP integration: application-specific SoC designs*
- *Strong roadmap*
  - *High-performance/power-efficient offerings*
  - *Moderate performance at lower power*
- *Architecture stability*
  - *IBM server offerings*
  - *Collaborative enhancements/extensions*
- *Vibrant ecosystem*
  - *Diverse and growing*
  - *Collaboration to address community needs*
- *Choice*
  - *Multiple application-specific integrated circuit (ASIC) and application-specific standard product (ASSP) suppliers*
  - *Route-to-market options (field-programmable grid array [FPGA], ASIC, ASSP)*
  - *Manufacturing flexibility*
  - *Freedom to innovate and differentiate*

Solving the performance needs of multiple markets

The PowerPC 476FP processor core is designed to meet the high-end and low-end demands of multiple market applications. By maintaining the Power instruction set architecture (ISA), existing code for set top boxes, game consoles, communication devices, and other embedded applications can adopt this core and meet the current performance requirements of these applications. The core leverages an extensive PowerPC ecosystem providing ready solutions on which customers can build their applications. The stability of the architecture ensures that, as applications grow, future derivatives can take advantage of the investment in an application code base, creating a model for reduced development spending. The ability to run multiple cores as part of an application allows the PowerPC 476FP processor core to scale from applications such as a uniprocessor mobile internet device to a network processor requiring multiple coherent cores on a single chip.



Peak performance

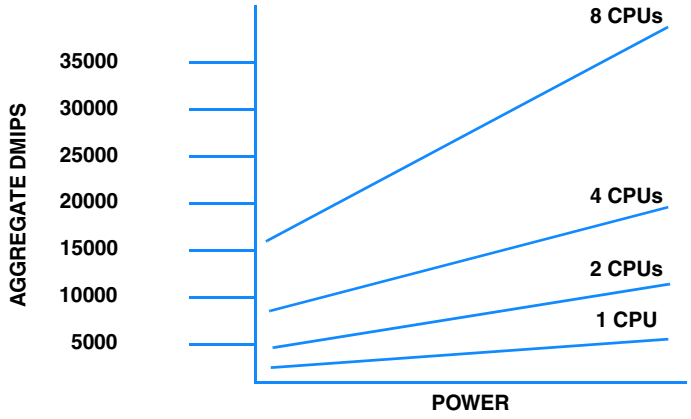
- *1.6 GHz+ capability delivers peak performance for uniprocessor designs*
- *Exceptional scalability, supporting up to eight coherent processors on a single PLB6 arbiter*

The PowerPC 476FP—a uniprocessor

Exceeding 1.6 GHz frequency, the PowerPC 476FP core is well positioned at the top of the performance/power pyramid for embedded designs—a unicore implementation that handles the growing performance needs of consumer media applications while extending its use in communications and mid-to-high-end multifunction printer applications.

The ability to use auxiliary engines such as a double-precision floating-point unit (FPU) further extends the versatility of this core.

Scaling performance through multiple-core designs



The PowerPC 476FP—a classic SMP processor

As a multiple-processor implementation, the core supports both SMP (symmetric multi-processing) and AMP (asymmetric multi-processing) operations.

SMP allows multiple processors to share common memory and work simultaneously without corrupting each other's work. When using the IBM PLB6 arbiter, applications can run simultaneously on up to 16 separate PowerPC 476FP processors (8 coherent) providing extended processing power to applications requiring it. With high throughput processing (depending on the application, up

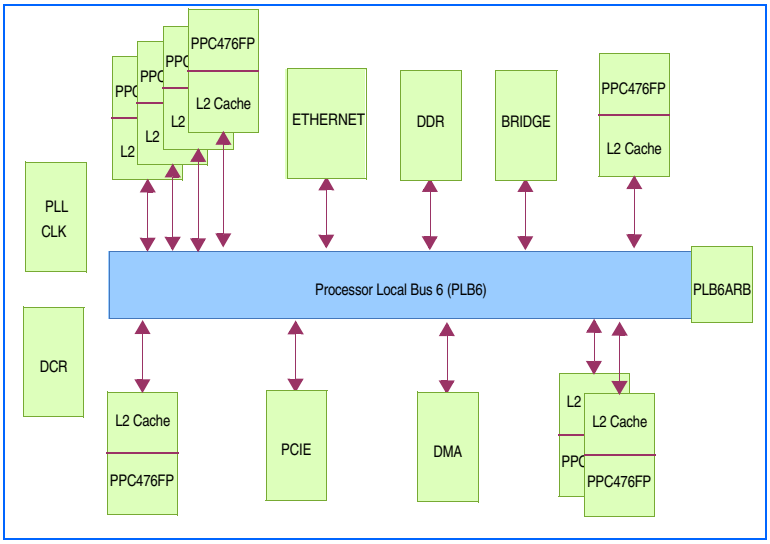
Code compatibility

- *Supports symmetric and asymmetric processing*
- *Minimizes power dissipation*
- *Handles a wide range of high-performance applications*
- *Shares common code with the PowerPC 4xx family of embedded controllers*

to 4750 DMIPS per core) this processor core can handle a wide range of high-performance applications. Manufacturing this core in IBM 45 nm silicon-on-insulator (SOI) technology results in products that can handle high-performance applications, yet remain best of breed in power dissipation against its competitive rivals.

Combining data plane and control plane functions in the communication space on a single SoC can readily be realized using this processor. The core can be connected to other PowerPC 4xx cores to optimize an application and minimize power dissipation while seamlessly running PowerPC code. The versatile PowerPC family of products, that start at a fraction of a mW/MHz for the PowerPC 405 core and extend to 1.6 GHz+ capability for the PowerPC 476FP core, can all be intermixed in a solution and all share common code. This provides a great range for customers of this family of products.

The following figure provides an example of an advanced SoC design solution.



Microarchitecture

- *Nine-stage, 5-issue, out-of-order issue, execution, and in-order completion*
- *Up to 32 instructions in flight*
- *Shadow general purpose registers to reduce execution stalling and simplify operand forwarding*
- *Little-endian support*
- *Speculative prefetching to the instruction cache*
- *Dynamic branch prediction with a branch history table and link stack*

Advanced microarchitecture

The PowerPC 476FP embedded processor core is a 5-issue, 4-pipeline, superscalar 32-bit reduced instruction set computer (RISC). The multiple integrated pipelines allow for out-of-order instruction execution, contributing to the overall performance increases of the processor. The specifications for the PowerPC 476FP core are shown in the following table.

Specifications	
Performance:* Dhrystone 2.1	2.5 DMIPS per MHz
Technology	IBM CMOS SOI 45 nm; eight metal layer utilization
Processor clock frequency*	1.6 GHz
Power dissipation (total)*	1.6 W (estimated)
Size*	3.6 mm^2
Availability	IBM ASIC Cu-45 hard core

* Preliminary estimates; subject to change

Execution unit

The PowerPC 476FP execution unit has four integrated pipelines. The load/store pipeline (L-Pipe) is implemented in the data cache controller. The integer pipeline (I-Pipe) provides for all arithmetic and logical operations, including multiply, divide, and system operations. The secondary integer pipeline (J-Pipe) provides for simple arithmetic and logical operations, and a dedicated branch pipeline (B-Pipe) is used for branch determination and execution. These pipelines allow out-of-order instruction execution but in-order completion, with up to 32 instructions in flight. The PowerPC architecture allows for accelerated integer multiply and multiply-accumulate (MAC) instructions, all of which are fully supported by the PowerPC 476FP core. The execution unit also provides a shadow array of the general purpose registers to reduce execution stalling and simplify operand forwarding. In addition, the execution unit provides both big-endian and little-endian support, SMP coherency support for load-with-reservation and store conditional operations, and dynamic branch prediction including a branch history table and link stack.

Flexibility and floating-point

- *Multiply-accumulate instructions included to provide additional flexibility and performance for digital signal processing (DSP) applications.*
- *Integrated single-precision and double-precision floating-point unit that supports dot form instructions to provide better performance for graphics and printer applications*

Floating-point unit

The FPU is a dedicated execution unit for performing mathematical operations on floating-point numbers. The FPU in the PowerPC 476FP core is a pipelined, scalar, double-precision floating-point unit that is decoupled from the CPU. The FPU supports both double-precision and single-precision ANSI/IEEE 754-1985 Floating-Point Standard operations. The FPU is Power ISA V2.05 compliant and implements all instructions in the PowerPC floating-point instruction set including the record form (also known as the dot form). The dot form of these arithmetic and logical operations update the Condition Register (CR). Previous PowerPC 4xx designs emulated the dot-form instructions in software. The FPU is superscalar; it has independent floating-point load/store and execution units, with extended operation stages for normal operation and extended divide stages.

Instruction and data caches

The PowerPC 476FP core provides separate instruction cache (I-cache) and data cache (D-cache) controllers and arrays. These controllers and arrays allow concurrent access and minimize pipeline stalls. The cache arrays are 32 KB each. Both cache controllers have 32-byte lines and are 4-way set associative. The PowerPC 476FP core also provides special debug instructions that can directly read the tag and data arrays. Both the instruction and data cache controllers interface to the level 2 (L2) cache. To provide redundancy and protection, both caches are parity protected. Any parity errors cause the processor to vector to the machine check interrupt handler where operating system software can take appropriate action. The read and write buses between the L1 and L2 caches are also parity protected.

Memory management unit

The PowerPC 476FP memory management unit (MMU) provides cache control, access protection, and address translation. It is a software managed unit with hardware assistance for writing or replacing entries when required. The MMU provides a 42-bit real address space supporting 4 TB, and a 49-bit virtual address space. The MMU contains a 1024-entry, 4-way, set-associative unified translation lookaside buffer (UTLB), and the control logic and register set that support it. The MMU divides the address space

Companion cores

- *L2 cache controller that supports memory coherency*
- *Processor local bus controller that supports coherent and non-coherent functional blocks*
- *DDR3 memory controller with coherent support*
- *Multi-processor interrupt controller*

(whether effective, virtual, or real) into pages. Seven page sizes of 4 KB, 16 KB, 64 KB, 1 MB, 16 MB, 256 MB, and 1 GB are supported simultaneously, such that at any given time the TLB can contain entries for any combination of page sizes. Each MMU entry can specify if the memory is to be addressed as big-endian or little-endian.

Timer facilities

The PowerPC 476FP processor core contains a time base and three timers: a decrementer (DEC), a fixed-interval timer (FIT), and a watchdog timer. The PowerPC 476FP core provides new timer divide selection logic, allowing the timer clock source (1.6 GHz) to be divided by 4, 8, or 16, greatly expanding the number of possible clock rates for the various timers.

Test and debug facilities

Like the other processor cores in the PowerPC 4xx family, the PowerPC 476FP core supports Joint Test Action Group (JTAG) interfaces that allow a low-level debugger to reset, stop, halt, and start the processor core, to trace the status and operation of one or more processor cores and other devices in the chip, and to perform other software and hardware debugging operations. These features greatly reduce application hardware and software debug times for faster time to market.

Companion logic

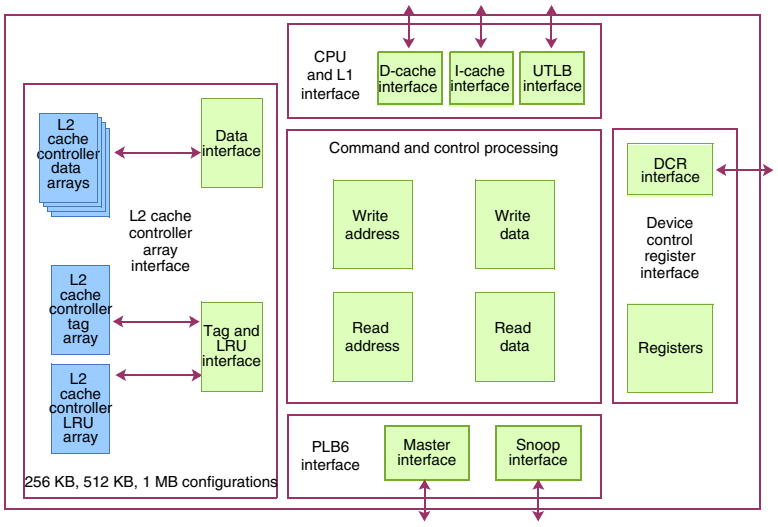
IBM maintains a standard intellectual property library containing a broad spectrum of circuit functions for easy integration into SoC designs. Balancing power and performance can become much less complicated by mixing and matching these elements to meet design goals. PowerPC 476FP designs might or might not use the L2 cache controller and processor local bus as part of the design.

L2 cache

- *256 KB, 512 KB, or 1 MB cache size*
- *128-byte cache line*
- *Four-way set-associative*
- *MESI+t+LS+MU cache state protocol*

L2 cache controller

The L2 cache controller is a companion core to the PowerPC 476FP core. Each instance of the L2 cache controller supports a single CPU core and manages transfers between the PowerPC 476FP level 1 (L1) instruction and data caches and the PLB6 SMP coherent memory subsystem. The L2 cache controller supports cache arrays of 256 KB, 512 KB, or 1 MB, each being organized as 4-way set-associative, and a 128-byte cache line. It is implemented as a write-back design, with an 8-entry write queue with store gathering for L1 cache stores. Another important feature of the L2 cache controller is error checking and correction (ECC) and parity protection. The controller provides single-error correcting, double-error detecting (SECDED) redundancy and error management on both the data and tag arrays. The controller also includes debug facilities accessed through a device control register (DCR) interface. In addition, interfaces to the PLB6 are parity-protected. The L2 cache subsystem can operate at 800 MHz. The interface between the CPU and L2 allows for different clock domains, with a maximum clock ratio of 2:1. The interface to the PLB6 can also be in a separate clock domain and can run at 1:1 or slower. The following figure shows the logical organization of the L2 cache controller.



Processor and I/O bus

- *SMP coherency with seven cache states*
- *Each attachment point includes a 128-bit read bus and a 128-bit write data bus*
- *Concurrent traffic on the read and write data bus*
- *Concurrent transfers on all segments*
- *Request pipelining*
- *Out-of-order read data*

Processor local bus 6

The PLB6 is a high-performance, on-chip system bus that supports coherency in multiple-core designs. It enables up to sixteen masters to be connected to up to eight slave segments, with up to four devices per segment. It is responsible for arbitration and routing between the masters and slave segments. The PLB6 supports 800 MHz clock frequency and can operate with the L2 cache controller at a 1:1 or slower ratio, and provides concurrent 128-bit read and write data buses. The PLB6 is a bus controller with eight segments, providing an aggregate bandwidth of 204.8 GB/s (25.6 GB/s $\times$ 8 segments). The PLB6 supports out-of-order read data. The bus ordering mechanism allows easy attachments to high-performance PCI-type devices and accelerates performance of write-followed-by-read transactions, regardless of passing-not-allowed dependency between them. For smaller applications, the PLB6 is configurable and can be instantiated using fewer ways.

Device control register bus

DCRs are on-chip registers that control various PowerPC 476FP system functions, such as the operation of PowerPC 476FP buses, peripherals, and certain CPU behaviors. The architected DCR bus is used to move data between general purpose registers (GPRs) and DCRs. The DCR bus off loads status and controls read and write transfers from the high-performance PLB. The DCR bus arbiter supports multiple processor applications.

Multi-processor interrupt controller

The MPIC core supports up to 128 individual interrupt sources with programmable interrupt priorities, interrupt vector assignment, and interrupt destination designation per interrupt source. Based on its priority, an interrupt source can cause the MPIC to output a machine check, critical interrupt, or noncritical interrupt. Each interrupt source is individually maskable. Priority based on interrupt masking (task priority) is also provided on a per processor basis. The MPIC core supports multi-processor environments by providing interprocessor/self interrupts, processor initialization control, distributed interrupt delivery, and directed interrupt delivery as required.

Available development tools

- *Instruction set simulator*
- *PowerPC 476FP Linux kernel*
- *GNU tool chain support, including optimized compiler*
- *Debuggers*
- *Bus Toolkit*
- *Documentation*

Tools and ecosystem

The PowerPC 476FP core is a member of the PowerPC 400 series of advanced embedded processor cores. To give third-party software tools and developers a head start, IBM has worked with many third-party vendors to offer a full range of robust development tools for embedded applications. Among these are compilers, debuggers, real-time operating systems, and logic analyzers.

To give software developers a jump-start on code development, IBM has enabled a full suite of development tools including a PowerPC 476FP-enabled instruction set simulator (ISS), which allows programmers to begin software development immediately.

The IBM Linux Technology Center (LTC) is an IBM team of open-source software developers who work in cooperation with the Linux open-source development community. Developers in the LTC have added support for the PowerPC 476FP core into the Linux kernel and the GNU tool chain, which includes GCC, GDB, and GAS.

Comprehensive documentation can be found in the IBM Technical Library (www.ibm.com/chips/techlib). Software and hardware support is provided by the IBM PowerPC applications engineering team, at ppcsupp@us.ibm.com.

Summary

The PowerPC 476FP core is a giant leap forward for IBM embedded processor cores. Based on the proven Power Architecture, an instruction set architecture that spans applications from consumer electronics to supercomputers, the PowerPC 476FP core incorporates features that provide enhanced functionality and unsurpassed performance. The PowerPC 476FP core has the performance, scalability, configuration flexibility, performance per milliwatt, ecosystem, and infrastructure to make it an attractive choice for many market segments.

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IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

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