

# PPC405CR

## PowerPC 405CR Embedded Processor

**Data Sheet**

### Features

- PowerPC® 405 32-bit RISC processor core operating up to 266MHz
  - Memory Management Unit
  - 16KB instruction and 8KB data caches
  - Multiply-Accumulate (MAC) function, including fast multiply unit
  - Programmable Timers
- Synchronous DRAM (SDRAM) interface operating up to 133MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, 16-, or 32-bit SRAM and external peripherals
  - Up to eight devices
  - External Mastering supported
- DMA support for external peripherals, internal UART and memory
  - Scatter-gather chaining supported
  - Four channels
- Programmable Interrupt Controller supports interrupts from a variety of sources
  - Supports 7 external and 10 internal interrupts
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
- Two serial ports (16550 compatible UART)
- One IIC interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency

### Description

The PowerPC 405CR (PPC405CR) is a 32-bit RISC embedded controller. High performance, peripheral integration, and low cost make the device ideal for wired communications, network printers, and other computing applications.

This device is an easy upgrade for systems based on PowerPC 403xx embedded processors, while providing a base for custom chip designs.

The controller is powered by a PPC405 embedded core. This core tightly couples a 266 MHz CPU, MMU, instruction and data caches, and debug logic. Fine-tuning of the core reduces data transfer overhead, minimizes pipeline stalls, and improves performance.

The PPC405CR employs the IBM CoreConnect™ bus architecture. This architecture, as implemented on the PPC405CR, consists of a 64-bit, 133-MHz Processor Local Bus (PLB) and a 32-bit, 66-MHz On-Chip Peripheral Bus (OPB). High-performance peripherals attach to the PLB and less performance-critical peripherals attach to the OPB.

Technology: CMOS SA-12E 0.25  $\mu\text{m}$  (0.18  $\mu\text{m}$   $L_{\text{eff}}$ )

Package: 27mm, 316-ball enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 0.8W, Maximum 2.0W at 200MHz.

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**Ordering, PVR, and JTAG Information**

| Product Name | Order Part Number <sup>1, 2</sup> | Processor Frequency | Package               | Rev Level | PVR Value  | JTAG ID    |
|--------------|-----------------------------------|---------------------|-----------------------|-----------|------------|------------|
| PPC405CR     | PPC405CR-3BC133C                  | 133MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3BC133CZ                 | 133MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC133C                  | 133MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC133CZ                 | 133MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3BC200C                  | 200MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3BC200CZ                 | 200MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC200C                  | 200MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC200CZ                 | 200MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3BC266C                  | 266MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3BC266CZ                 | 266MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC266C                  | 266MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |
| PPC405CR     | PPC405CR-3KC266CZ                 | 266MHz              | 27mm, 316 ball E-PBGA | C         | 0x40110145 | 0x42051049 |

**Notes:** 1. Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.  
 2. Package type B contains lead; package type K is lead-free.

This section provides the part numbering nomenclature for the PPC405CR. For availability, contact your local AMCC sales office.

Each part number contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the *PPC405CR Embedded Processor User's Manual* for details on the register content.

**Part Number Key**

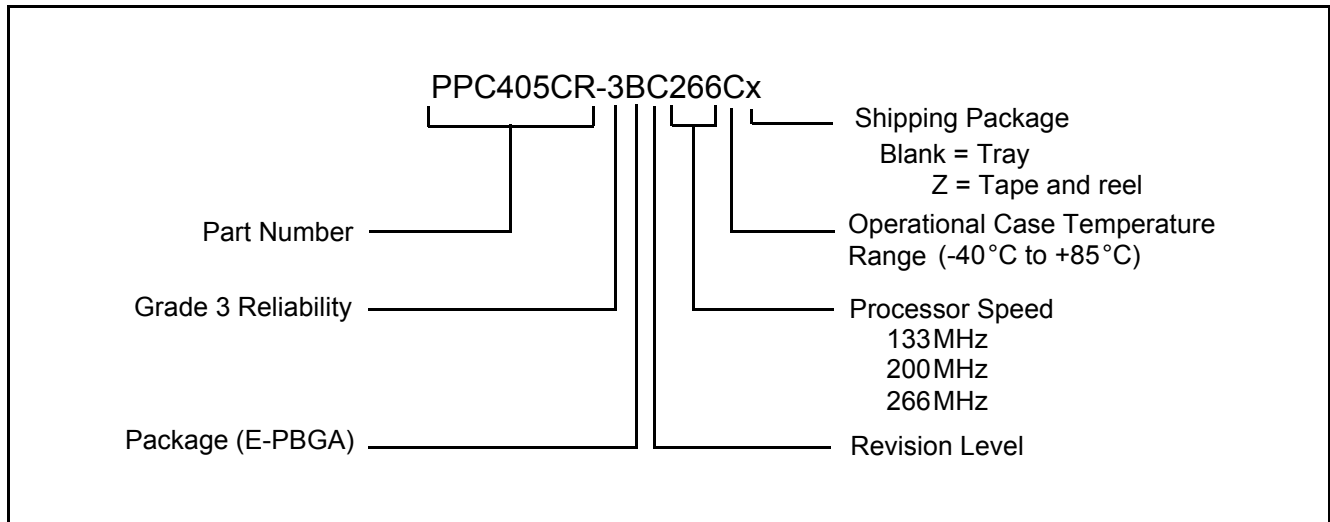
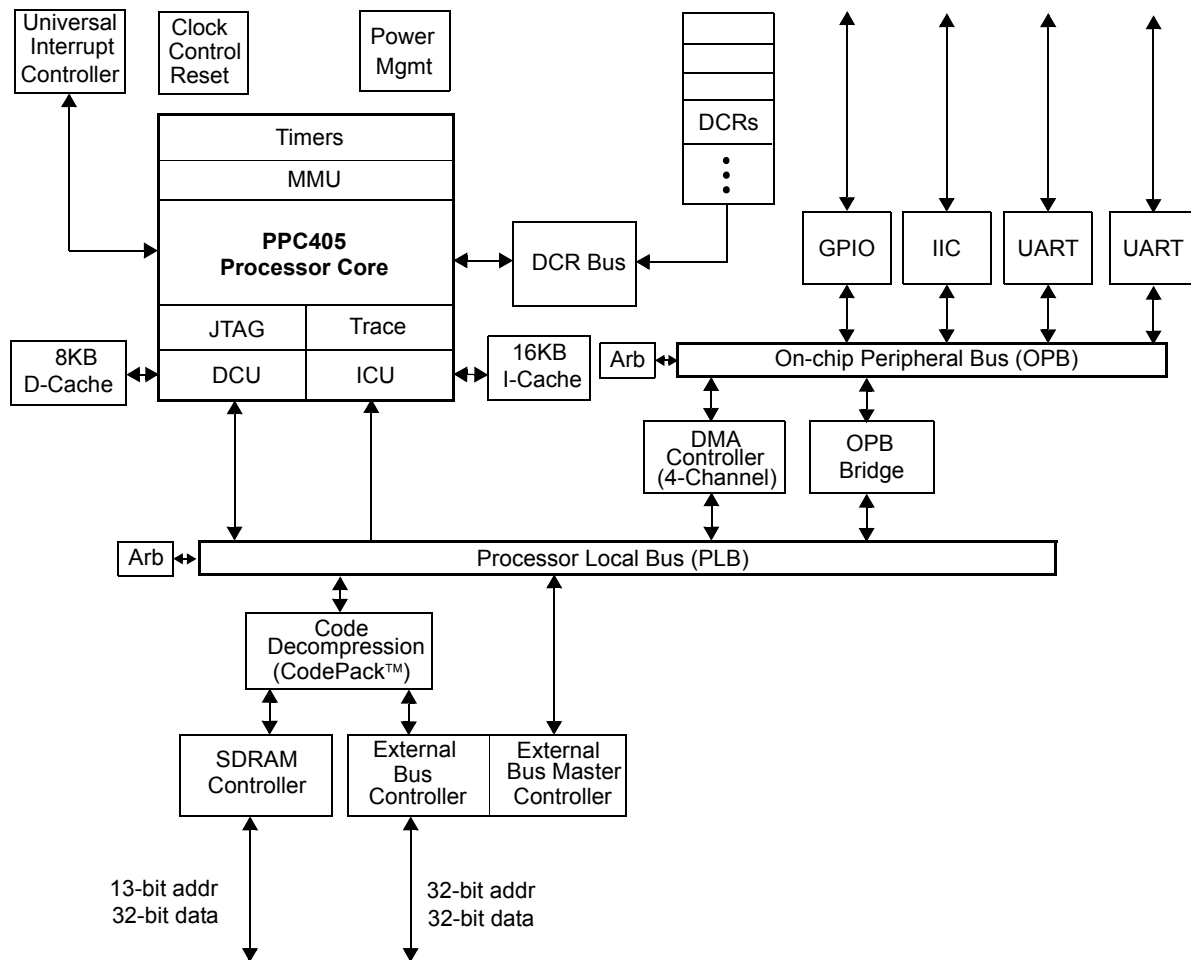


Figure 1. PPC405CR Embedded Controller Functional Block Diagram



The PPC405CR is designed using the IBM Microelectronics Blue Logic<sup>®</sup> methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect<sup>™</sup> Bus Architecture.

## Address Map Support

The PPC405CR incorporates two simple and separate address maps. The first address map defines the possible use of address regions that the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC405CR processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (4GB System Memory)

| Function             | Subfunction   | Start Address | End Address  | Size   |
|----------------------|---|---------------|--------------|--------|
| General Use          | SDRAM and External Peripherals<br><b>Note:</b> Any of the address ranges listed at right may be use for any of the above functions. | 0x00000000    | 0xEF5FFFFFFF | 3830MB |
|                      |   | 0xF0000000    | 0xFFFFFFFF   | 256MB  |
| Boot-up              | Peripheral Bus Boot <sup>1</sup>  | 0xFFE00000    | 0xFFFFFFFF   | 2MB    |
| Internal Peripherals | UART0   | 0xEF600300    | 0xEF600307   | 8B     |
|                      | UART1   | 0xEF600400    | 0xEF600407   | 8B     |
|                      | IIC0  | 0xEF600500    | 0xEF60051F   | 32B    |
|                      | OPB Arbiter   | 0xEF600600    | 0xEF60063F   | 64B    |
|                      | GPIO Controller Registers   | 0xEF600700    | 0xEF60077F   | 128B   |

**Notes:**

1. When peripheral bus boot is selected, Peripheral bank 0 is automatically configured at reset to the address range listed above.
2. After the boot process, software may reassign the boot memory region for other uses.
3. All address ranges not listed above are reserved.

Table 2. DCR Address Map

| Function                                   | Start Address | End Address | Size                   |
|--|---------------|-------------|------------------------|
| <b>Total DCR Address Space<sup>1</sup></b> | 0x000         | 0x3FF       | 1KW (4KB) <sup>1</sup> |
| Reserved                                   | 0x000         | 0x00F       | 16W                    |
| Memory Controller Registers                | 0x010         | 0x011       | 2W                     |
| External Bus Controller Registers          | 0x012         | 0x013       | 2W                     |
| Decompression Controller Registers         | 0x014         | 0x015       | 2W                     |
| Reserved                                   | 0x016         | 0x07F       | 106W                   |
| PLB Registers                              | 0x080         | 0x08F       | 16W                    |
| Reserved                                   | 0x090         | 0x09F       | 16W                    |
| OPB Bridge Out Registers                   | 0x0A0         | 0x0A7       | 8W                     |
| Reserved                                   | 0x0A8         | 0x0AF       | 8W                     |
| Clock, Control, and Reset                  | 0x0B0         | 0x0B7       | 8W                     |
| Power Management                           | 0x0B8         | 0x0BF       | 8W                     |
| Interrupt Controller                       | 0x0C0         | 0x0CF       | 16W                    |
| Reserved                                   | 0x0D0         | 0x0FF       | 48W                    |
| DMA Controller Registers                   | 0x100         | 0x13F       | 64W                    |
| Reserved                                   | 0x140         | 0x3FF       | 704W                   |

**Notes:**

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

## SDRAM Memory Controller

The PPC405CR Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256 MB per bank are supported, up to a maximum of 1 GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- 32-bit memory interface support
- Programmable address compare for each bank of memory
- Industry standard 168-pin DIMMS are supported (some configurations)
- 4 MB to 256 MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page mode accesses with up to 4 open pages
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging

## External Peripheral Bus Controller (EBC)

- Supports eight banks of ROM, EPROM, SRAM, Flash memory, or slave peripheral I/O
- Up to 66 MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 0–255 wait states for non-burst devices
  - 0–31 burst wait states for first access and up to 7 wait states for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEOff (0 to 3 clock cycles) relative to CS
- Programmable address mapping
- Peripheral device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

## DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers

- Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

## UART

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

## IIC Bus Interface

- Compliant with Phillips® Semiconductors I<sup>2</sup>C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V<sub>DD</sub> IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

## General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- All GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. The 23 GPIOs are multiplexed with:
  - 7 of 8 chip selects.
  - All seven external interrupts.
  - All nine instruction trace pins.
- Each GPIO output is separately programmable to emulate an open-drain driver (two states, drive to zero or open circuit).



## Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

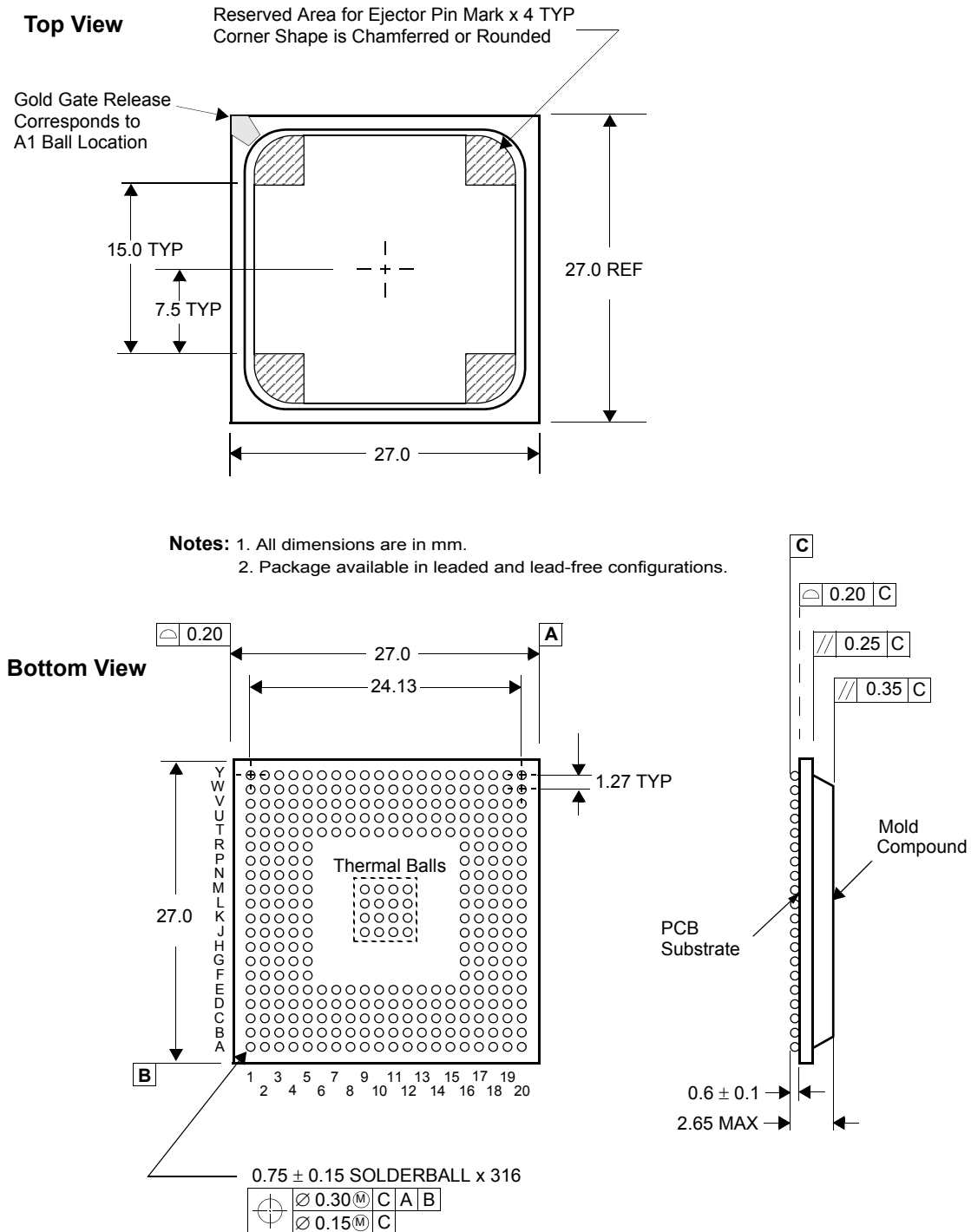
Features include:

- Supports 7 external and 10 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

## JTAG

- IEEE 1149.1 test access port
- IBM RISCWatch debugger support
- JTAG Boundary Scan Description Language (BSDL)

Figure 2. 27mm, 316-Ball E-PBGA Package



**Pin Lists**

In this section there are two tables that correlate the external signals to the physical package pin (ball) on which they appear.

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. The page number listed gives the page in “Signal Functional Description” on page 23 where the signals in the indicated interface group begin.

*Table 3. Signals Listed Alphabetically (Sheet 1 of 7)*

| Signal Name  | Ball   | Interface Group            | Page |
|--|--|----------------------------|------|
| AV <sub>DD</sub>   | E20  | Power                      | 27   |
| BA0<br>BA1   | J17<br>H18   | SDRAM                      | 23   |
| <u>BankSel0</u><br><u>BankSel1</u><br><u>BankSel2</u><br><u>BankSel3</u> | L19<br>N17<br>P17<br>U19                             | SDRAM                      | 23   |
| BusReq   | P2   | External Master Peripheral | 25   |
| <u>CAS</u>   | K17  | SDRAM                      | 23   |
| ClkEn0<br>ClkEn1   | J19<br>G20   | SDRAM                      | 23   |
| DMAAck0<br>DMAAck1<br>DMAAck2<br>DMAAck3                                 | C16<br>B17<br>B16<br>A14                             | External Slave Peripheral  | 23   |
| DMAReq0<br>DMAReq1<br>DMAReq2<br>DMAReq3                                 | A19<br>C15<br>B15<br>A8                              | External Slave Peripheral  | 23   |
| DQM0<br>DQM1<br>DQM2<br>DQM3   | U18<br>W14<br>Y10<br>U8                              | SDRAM                      | 23   |
| DQMCB  | V19  | SDRAM                      | 23   |
| Drvrlnh1<br>Drvrlnh2   | F17<br>C19   | System                     | 26   |
| ECC0<br>ECC1<br>ECC2<br>ECC3<br>ECC4<br>ECC5<br>ECC6<br>ECC7             | V17<br>Y18<br>U14<br>V13<br>Y13<br>V12<br>W11<br>V11 | SDRAM                      | 23   |
| EOT0/TC0<br>EOT1/TC1<br>EOT2/TC2<br>EOT3/TC3                             | G4<br>F2<br>W1<br>Y2                                 | External Slave Peripheral  | 23   |
| <u>ExtAck</u><br><u>ExtReq</u><br><u>ExtReset</u>                        | U5<br>Y3<br>P4                                       | External Master Peripheral | 25   |

Table 3. Signals Listed Alphabetically (Sheet 2 of 7)

| Signal Name | Ball | Interface Group  | Page |
|-------------|------|--|------|
| GND         | A1   | Power<br><b>Note:</b> J9–J12, K9–K12, L9–L12, and M9–M12 are also thermal balls. | 27   |
|             | A6   |  |      |
|             | A10  |  |      |
|             | A15  |  |      |
|             | A20  |  |      |
|             | B2   |  |      |
|             | B19  |  |      |
|             | C3   |  |      |
|             | C18  |  |      |
|             | D4   |  |      |
|             | D17  |  |      |
|             | E5   |  |      |
|             | E10  |  |      |
|             | E11  |  |      |
|             | E16  |  |      |
|             | F1   |  |      |
|             | F20  |  |      |
|             | J9   |  |      |
|             | J10  |  |      |
|             | J11  |  |      |
| J12         |      |  |      |
| K5          |      |  |      |
| K9          |      |  |      |
| K10         |      |  |      |
| K11         |      |  |      |
| K12         |      |  |      |
| K16         |      |  |      |
| K20         |      |  |      |
| L1          |      |  |      |
| L5          |      |  |      |
| L9          |      |  |      |
| L10         |      |  |      |
| L11         |      |  |      |
| L12         |      |  |      |
| L16         |      |  |      |
| M9          |      |  |      |
| M10         |      |  |      |
| M11         |      |  |      |
| M12         |      |  |      |
| R1          |      |  |      |
| R20         |      |  |      |
| GND (cont)  | T5   | Power  | 27   |
|             | T10  |  |      |
|             | T11  |  |      |
|             | T16  |  |      |
|             | U4   |  |      |
|             | U17  |  |      |
|             | V3   |  |      |
|             | V18  |  |      |
|             | W2   |  |      |
|             | W19  |  |      |
|             | Y1   |  |      |
|             | Y6   |  |      |
|             | Y11  |  |      |
|             | Y15  |  |      |
| Y20         |      |  |      |

Table 3. Signals Listed Alphabetically (Sheet 3 of 7)

| Signal Name   | Ball   | Interface Group   | Page |
|---|--|---|------|
| GPIO1[TS1E]<br>GPIO2[TS2E]<br>GPIO3[TS1O]<br>GPIO4[TS2O]<br>GPIO5[TS3]<br>GPIO6[TS4]<br>GPIO7[TS5]<br>GPIO8[TS6]<br>GPIO9[TrcClk]                           | B18<br>D16<br>C17<br>P18<br>T17<br>W18<br>Y19<br>W13<br>V6                 | System  | 26   |
| Halt  | E19  | System  | 26   |
| HoldAck<br>HoldPri<br>HoldReq   | T4<br>T3<br>V2   | External Master Peripheral  | 25   |
| IIC_SCL   | U15  | Internal Peripheral   | 25   |
| IIC_SDA   | W17  | Internal Peripheral   | 25   |
| IRQ0[GPIO17]<br>IRQ1[GPIO18]<br>IRQ2[GPIO19]<br>IRQ3[GPIO20]<br>IRQ4[GPIO21]<br>IRQ5[GPIO22]<br>IRQ6[GPIO23]  | D18<br>C20<br>E18<br>D20<br>G17<br>F18<br>W20                              | Interrupts  | 26   |
| MemAddr0<br>MemAddr1<br>MemAddr2<br>MemAddr3<br>MemAddr4<br>MemAddr5<br>MemAddr6<br>MemAddr7<br>MemAddr8<br>MemAddr9<br>MemAddr10<br>MemAddr11<br>MemAddr12 | Y7<br>W7<br>V8<br>U7<br>Y4<br>U6<br>W4<br>V5<br>W3<br>V4<br>U3<br>V1<br>T2 | SDRAM<br><b>Note:</b> During a $\overline{\text{CAS}}$ cycle MemAddr0 is the least significant bit (lsb) on this bus. | 23   |
| MemClkOut0<br>MemClkOut1  | H20<br>G18   | SDRAM   | 23   |

Table 3. Signals Listed Alphabetically (Sheet 4 of 7)

| Signal Name      | Ball   | Interface Group   | Page |
|------------------|--|---|------|
| MemData0         | J18  | SDRAM<br><b>Note:</b> MemData0 is the most significant bit (msb) on this bus. | 23   |
| MemData1         | K19  |   |      |
| MemData2         | L20  |   |      |
| MemData3         | M20  |   |      |
| MemData4         | M19  |   |      |
| MemData5         | L18  |   |      |
| MemData6         | L17  |   |      |
| MemData7         | N20  |   |      |
| MemData8         | N19  |   |      |
| MemData9         | M18  |   |      |
| MemData10        | M17  |   |      |
| MemData11        | P20  |   |      |
| MemData12        | P19  |   |      |
| MemData13        | N18  |   |      |
| MemData14        | U20  |   |      |
| MemData15        | T18  |   |      |
| MemData16        | W16  |   |      |
| MemData17        | Y17  |   |      |
| MemData18        | Y16  |   |      |
| MemData19        | V14  |   |      |
| MemData20        | Y14  |   |      |
| MemData21        | U12  |   |      |
| MemData22        | W12  |   |      |
| MemData23        | Y12  |   |      |
| MemData24        | Y9   |   |      |
| MemData25        | W9   |   |      |
| MemData26        | V10  |   |      |
| MemData27        | U10  |   |      |
| MemData28        | Y8   |   |      |
| MemData29        | W8   |   |      |
| MemData30        | V9   |   |      |
| MemData31        | U9   |   |      |
| OV <sub>DD</sub> | F5<br>G5<br>P5<br>R5<br>T6<br>T7<br>T14<br>T15<br>F16<br>G16<br>P16<br>R16<br>E6<br>E7<br>E14<br>E15 | Power   | 27   |

Table 3. Signals Listed Alphabetically (Sheet 5 of 7)

| Signal Name    | Ball | Interface Group   | Page |
|----------------|------|---|------|
| PerAddr0       | A3   | External Slave Peripheral<br><b>Note:</b> PerAddr0 is the most significant bit (msb) on this bus. | 23   |
| PerAddr1       | A4   |   |      |
| PerAddr2       | B6   |   |      |
| PerAddr3       | D7   |   |      |
| PerAddr4       | C6   |   |      |
| PerAddr5       | B7   |   |      |
| PerAddr6       | D8   |   |      |
| PerAddr7       | C7   |   |      |
| PerAddr8       | B8   |   |      |
| PerAddr9       | A7   |   |      |
| PerAddr10      | D9   |   |      |
| PerAddr11      | C8   |   |      |
| PerAddr12      | B9   |   |      |
| PerAddr13      | D10  |   |      |
| PerAddr14      | C9   |   |      |
| PerAddr15      | A9   |   |      |
| PerAddr16      | B11  |   |      |
| PerAddr17      | A11  |   |      |
| PerAddr18      | B12  |   |      |
| PerAddr19      | D11  |   |      |
| PerAddr20      | A13  |   |      |
| PerAddr21      | B13  |   |      |
| PerAddr22      | C12  |   |      |
| PerAddr23      | D12  |   |      |
| PerAddr24      | B14  |   |      |
| PerAddr25      | C13  |   |      |
| PerAddr26      | D13  |   |      |
| PerAddr27      | A16  |   |      |
| PerAddr28      | C14  |   |      |
| PerAddr29      | D14  |   |      |
| PerAddr30      | A17  |   |      |
| PerAddr31      | D15  |   |      |
| PerBLast       | E2   | External Slave Peripheral   | 23   |
| PerClk         | D3   | External Master Peripheral  | 25   |
| PerCS0         | D6   | External Slave Peripheral   | 23   |
| PerCS1[GPIO10] | B5   |   |      |
| PerCS2[GPIO11] | C5   |   |      |
| PerCS3[GPIO12] | A5   |   |      |
| PerCS4[GPIO13] | B10  |   |      |
| PerCS5[GPIO14] | C10  |   |      |
| PerCS6[GPIO15] | A12  |   |      |
| PerCS7[GPIO16] | C11  |   |      |

Table 3. Signals Listed Alphabetically (Sheet 6 of 7)

| Signal Name | Ball                            | Interface Group  | Page |
|-------------|---------------------------------|--|------|
| PerData0    | U2                              | External Slave Peripheral<br><b>Note:</b> PerData0 is the most significant bit (msb) on this bus.  | 23   |
| PerData1    | R4                              |  |      |
| PerData2    | U1                              |  |      |
| PerData3    | R2                              |  |      |
| PerData4    | R3                              |  |      |
| PerData5    | T1                              |  |      |
| PerData6    | N4                              |  |      |
| PerData7    | P3                              |  |      |
| PerData8    | N2                              |  |      |
| PerData9    | P1                              |  |      |
| PerData10   | M4                              |  |      |
| PerData11   | N3                              |  |      |
| PerData12   | M2                              |  |      |
| PerData13   | N1                              |  |      |
| PerData14   | L4                              |  |      |
| PerData15   | M3                              |  |      |
| PerData16   | L2                              |  |      |
| PerData17   | M1                              |  |      |
| PerData18   | K2                              |  |      |
| PerData19   | L3                              |  |      |
| PerData20   | K1                              |  |      |
| PerData21   | J1                              |  |      |
| PerData22   | J2                              |  |      |
| PerData23   | K3                              |  |      |
| PerData24   | K4                              |  |      |
| PerData25   | H1                              |  |      |
| PerData26   | H2                              |  |      |
| PerData27   | J3                              |  |      |
| PerData28   | J4                              |  |      |
| PerData29   | G1                              |  |      |
| PerData30   | G2                              |  |      |
| PerData31   | H3                              |  |      |
| PerErr      | B1                              | External Master Peripheral   | 25   |
| PerOE       | E4                              | External Slave Peripheral  | 23   |
| PerPar0     | C2                              | External Slave Peripheral  | 23   |
| PerPar1     | G3                              |  |      |
| PerPar2     | E1                              |  |      |
| PerPar3     | H4                              |  |      |
| PerReady    | E3                              | External Slave Peripheral  | 23   |
| PerR/W      | C1                              | External Slave Peripheral  | 23   |
| PerWBE0     | D2                              | External Slave Peripheral  | 23   |
| PerWBE1     | F4                              |  |      |
| PerWBE2     | F3                              |  |      |
| PerWBE3     | D1                              |  |      |
| PerWE       | C4                              | External Slave Peripheral  | 23   |
| RAS         | K18                             | SDRAM  | 23   |
| RcvrInh     | E17                             | System   | 26   |
| Reserved    | J20<br>G19<br>R17<br>T20<br>V16 | Other pins<br><b>Notes:</b><br>1. Connect G19 to ground.<br>2. Other reserved pins are not connected internally within the chip and should not have signals, voltage, or ground applied to them. | 27   |



Table 3. Signals Listed Alphabetically (Sheet 7 of 7)

| Signal Name   | Ball   | Interface Group     | Page |
|---|--|---------------------|------|
| SysClk<br>SysErr<br>SysReset  | H17<br>A18<br>D19  | System              | 26   |
| TCK<br>TDI<br>TDO   | B4<br>A2<br>D5   | JTAG                | 26   |
| TestEn  | F19  | System              | 26   |
| TmrClk  | B20  | System              | 26   |
| TMS   | B3   | JTAG                | 26   |
| TRST  | H19  | JTAG                | 26   |
| UART0_CTS<br>UART0_DCD<br>UART0_DSR<br>UART0_DTR<br>UART0_RI<br>UART0_RTS<br>UART0_Rx<br>UART0_Tx | W10<br>R18<br>U16<br>U13<br>V15<br>V20<br>T19<br>W15   | Internal Peripheral | 25   |
| UART1_DSR[UART1_CTS]<br>UART1_RTS[UART1_DTR]<br>UART1_Rx<br>UART1_Tx                              | V7<br>W6<br>W5<br>Y5   | Internal Peripheral | 25   |
| UARTSerClk  | R19  | Internal Peripheral | 25   |
| V <sub>DD</sub>   | E8<br>E9<br>E12<br>E13<br>H5<br>H16<br>J5<br>J16<br>M5<br>M16<br>N5<br>N16<br>T8<br>T9<br>T12<br>T13 | Power               | 27   |
| WE  | U11  | SDRAM               | 23   |

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 3)

| Ball | Signal Name                         | Ball | Signal Name                         | Ball | Signal Name                  | Ball | Signal Name                 |
|------|-------------------------------------|------|-------------------------------------|------|------------------------------|------|-----------------------------|
| A1   | GND                                 | B10  | PerCS4[GPIO13]                      | C19  | DrvrInh2                     | E8   | V <sub>DD</sub>             |
| A2   | TDI                                 | B11  | PerAddr16                           | C20  | IRQ1[GPIO18]                 | E9   | V <sub>DD</sub>             |
| A3   | PerAddr0                            | B12  | PerAddr18                           | D1   | $\overline{\text{PerWBE3}}$  | E10  | GND                         |
| A4   | PerAddr1                            | B13  | PerAddr21                           | D2   | $\overline{\text{PerWBE0}}$  | E11  | GND                         |
| A5   | $\overline{\text{PerCS3}}$ [GPIO12] | B14  | PerAddr24                           | D3   | PerClk                       | E12  | V <sub>DD</sub>             |
| A6   | Gnd                                 | B15  | DMAReq2                             | D4   | GND                          | E13  | V <sub>DD</sub>             |
| A7   | PerAddr9                            | B16  | DMAAck2                             | D5   | TDO                          | E14  | OV <sub>DD</sub>            |
| A8   | DMAReq3                             | B17  | DMAAck1                             | D6   | $\overline{\text{PerCS0}}$   | E15  | OV <sub>DD</sub>            |
| A9   | PerAddr15                           | B18  | GPIO1[TS1E]                         | D7   | PerAddr3                     | E16  | GND                         |
| A10  | GND                                 | B19  | GND                                 | D8   | PerAddr6                     | E17  | Rcrvinh                     |
| A11  | PerAddr17                           | B20  | TmrClk                              | D9   | PerAddr10                    | E18  | IRQ2[GPIO19]                |
| A12  | $\overline{\text{PerCS6}}$ [GPIO15] | C1   | PerR/W                              | D10  | PerAddr13                    | E19  | $\overline{\text{Halt}}$    |
| A13  | PerAddr20                           | C2   | PerPar0                             | D11  | PerAddr19                    | E20  | AV <sub>DD</sub>            |
| A14  | DMAAck3                             | C3   | GND                                 | D12  | PerAddr23                    | F1   | GND                         |
| A15  | GND                                 | C4   | $\overline{\text{PerWE}}$           | D13  | PerAdd26                     | F2   | EOT1/TC1                    |
| A16  | PerAddr27                           | C5   | $\overline{\text{PerCS2}}$ [GPIO11] | D14  | PerAddr29                    | F3   | $\overline{\text{PerWBE2}}$ |
| A17  | PerAddr30                           | C6   | PerAddr4                            | D15  | PerAddr31                    | F4   | $\overline{\text{PerWBE1}}$ |
| A18  | SysErr                              | C7   | PerAddr7                            | D16  | GPIO2[TS2E]                  | F5   | OV <sub>DD</sub>            |
| A19  | DMAReq0                             | C8   | PerAddr11                           | D17  | GND                          | F16  | OV <sub>DD</sub>            |
| A20  | GND                                 | C9   | PerAddr14                           | D18  | IRQ0[GPIO17]                 | F17  | DrvrInh1                    |
| B1   | PerErr                              | C10  | $\overline{\text{PerCS5}}$ [GPIO14] | D19  | $\overline{\text{SysReset}}$ | F18  | IRQ5[GPIO22]                |
| B2   | GND                                 | C11  | $\overline{\text{PerCS7}}$ [GPIO16] | D20  | IRQ3[GPIO20]                 | F19  | TestEn                      |
| B3   | TMS                                 | C12  | PerAddr22                           | E1   | PerPar2                      | F20  | GND                         |
| B4   | TCK                                 | C13  | PerAddr25                           | E2   | $\overline{\text{PerBLast}}$ | G1   | PerData29                   |
| B5   | $\overline{\text{PerCS1}}$ [GPIO10] | C14  | PerAddr28                           | E3   | PerReady                     | G2   | PerData30                   |
| B6   | PerAddr2                            | C15  | DMAReq1                             | E4   | $\overline{\text{PerOE}}$    | G3   | PerPar1                     |
| B7   | PerAddr5                            | C16  | DMAAck0                             | E5   | GND                          | G4   | EOT0/TC0                    |
| B8   | PerAddr8                            | C17  | GPIO3[TS10]                         | E6   | OV <sub>DD</sub>             | G5   | OV <sub>DD</sub>            |
| B9   | PerAddr12                           | C18  | GND                                 | E7   | OV <sub>DD</sub>             | G16  | OV <sub>DD</sub>            |

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 3)

| Ball | Signal Name              | Ball | Signal Name                  | Ball | Signal Name                  | Ball | Signal Name                    |
|------|--------------------------|------|------------------------------|------|------------------------------|------|--------------------------------|
| G17  | IRQ4[GPIO21]             | K2   | PerData18                    | M3   | PerData15                    | P18  | GPIO4[TS20]                    |
| G18  | MemClkOut1               | K3   | PerData23                    | M4   | PerData10                    | P19  | MemData12                      |
| G19  | Reserved                 | K4   | PerData24                    | M5   | V <sub>DD</sub>              | P20  | MemData11                      |
| G20  | ClkEn1                   | K5   | GND                          | M9   | Thermal Ball                 | R1   | GND                            |
| H1   | PerData25                | K9   | Thermal Ball                 | M10  | Thermal Ball                 | R2   | PerData3                       |
| H2   | PerData26                | K10  | Thermal Ball                 | M11  | Thermal Ball                 | R3   | PerData4                       |
| H3   | PerData31                | K11  | Thermal Ball                 | M12  | Thermal Ball                 | R4   | PerData1                       |
| H4   | PerPar3                  | K12  | Thermal Ball                 | M16  | V <sub>DD</sub>              | R5   | OV <sub>DD</sub>               |
| H5   | V <sub>DD</sub>          | K16  | GND                          | M17  | MemData10                    | R16  | OV <sub>DD</sub>               |
| H16  | V <sub>DD</sub>          | K17  | $\overline{\text{CAS}}$      | M18  | MemData9                     | R17  | Reserved                       |
| H17  | SysClk                   | K18  | $\overline{\text{RAS}}$      | M19  | MemData4                     | R18  | $\overline{\text{UART0\_DCD}}$ |
| H18  | BA1                      | K19  | MemData1                     | M20  | MemData3                     | R19  | UARTSerClk                     |
| H19  | $\overline{\text{TRST}}$ | K20  | GND                          | N1   | PerData13                    | R20  | GND                            |
| H20  | MemClkOut0               | L1   | GND                          | N2   | PerData8                     | T1   | PerData5                       |
| J1   | PerData21                | L2   | PerData16                    | N3   | PerData11                    | T2   | MemAddr12                      |
| J2   | PerData22                | L3   | PerData19                    | N4   | PerData6                     | T3   | HoldPri                        |
| J3   | PerData27                | L4   | PerData14                    | N5   | V <sub>DD</sub>              | T4   | HoldAck                        |
| J4   | PerData28                | L5   | GND                          | N16  | V <sub>DD</sub>              | T5   | GND                            |
| J5   | V <sub>DD</sub>          | L9   | Thermal Ball                 | N17  | $\overline{\text{BankSel1}}$ | T6   | OV <sub>DD</sub>               |
| J9   | Thermal Ball             | L10  | Thermal Ball                 | N18  | MemData13                    | T7   | OV <sub>DD</sub>               |
| J10  | Thermal Ball             | L11  | Thermal Ball                 | N19  | MemData8                     | T8   | V <sub>DD</sub>                |
| J11  | Thermal Ball             | L12  | Thermal Ball                 | N20  | MemData7                     | T9   | V <sub>DD</sub>                |
| J12  | Thermal Ball             | L16  | GND                          | P1   | PerData9                     | T10  | GND                            |
| J16  | V <sub>DD</sub>          | L17  | MemData6                     | P2   | BusReq                       | T11  | GND                            |
| J17  | BA0                      | L18  | MemData5                     | P3   | PerData7                     | T12  | V <sub>DD</sub>                |
| J18  | MemData0                 | L19  | $\overline{\text{BankSel0}}$ | P4   | $\overline{\text{ExtReset}}$ | T13  | V <sub>DD</sub>                |
| J19  | ClkEn0                   | L20  | MemData2                     | P5   | OV <sub>DD</sub>             | T14  | OV <sub>DD</sub>               |
| J20  | Reserved                 | M1   | PerData17                    | P16  | OV <sub>DD</sub>             | T15  | OV <sub>DD</sub>               |
| K1   | PerData20                | M2   | PerData12                    | P17  | $\overline{\text{BankSel2}}$ | T16  | GND                            |

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 3)

| Ball | Signal Name | Ball | Signal Name              | Ball | Signal Name              | Ball | Signal Name  |
|------|-------------|------|--------------------------|------|--------------------------|------|--------------|
| T17  | GPIO5[TS3]  | U18  | DQM0                     | V19  | DQMCB                    | W20  | IRQ6[GPIO23] |
| T18  | MemData15   | U19  | BankSel3                 | V20  | UART0_RTS                | Y1   | GND          |
| T19  | UART0_RX    | U20  | MemData14                | W1   | EOT2/TC2                 | Y2   | EOT3/TC3     |
| T20  | Reserved    | V1   | MemAddr11                | W2   | GND                      | Y3   | ExtReq       |
| U1   | PerData2    | V2   | HoldReq                  | W3   | MemAddr8                 | Y4   | MemAddr4     |
| U2   | PerData0    | V3   | GND                      | W4   | MemAddr6                 | Y5   | UART1_TX     |
| U3   | MemAddr10   | V4   | MemAddr9                 | W5   | UART1_RX                 | Y6   | GND          |
| U4   | GND         | V5   | MemAddr7                 | W6   | UART1_RTS<br>[UART1_DTR] | Y7   | MemAddr0     |
| U5   | ExtAck      | V6   | GPIO9[TrcClk]            | W7   | MemAddr1                 | Y8   | MemData28    |
| U6   | MemAddr5    | V7   | UART1_DSR<br>[UART1_CTS] | W8   | MemData29                | Y9   | MemData24    |
| U7   | MemAddr3    | V8   | MemAddr2                 | W9   | MemData25                | Y10  | DQM2         |
| U8   | DQM3        | V9   | MemData30                | W10  | UART0_CTS                | Y11  | GND          |
| U9   | MemData31   | V10  | MemData26                | W11  | ECC6                     | Y12  | MemData23    |
| U10  | MemData27   | V11  | ECC7                     | W12  | MemData22                | Y13  | ECC4         |
| U11  | WE          | V12  | ECC5                     | W13  | GPIO8[TS6]               | Y14  | MemData20    |
| U12  | MemData21   | V13  | ECC3                     | W14  | DQM1                     | Y15  | GND          |
| U13  | UART0_DTR   | V14  | MemData19                | W15  | UART0_TX                 | Y16  | MemData18    |
| U14  | ECC2        | V15  | UART0_RI                 | W16  | MemData16                | Y17  | MemData17    |
| U15  | IIC_SCL     | V16  | Reserved                 | W17  | IIC_SDA                  | Y18  | ECC1         |
| U16  | UART0_DSR   | V17  | ECC0                     | W18  | GPIO6[TS4]               | Y19  | GPIO7[TS5]   |
| U17  | GND         | V18  | GND                      | W19  | GND                      | Y20  | GND          |

## Signal Descriptions

The PPC405CR embedded controller is packaged in a 316-ball enhanced plastic ball grid array (E-PBGA). The following table provides a summary of the number of package pins associated with each functional interface group.

Table 5. Pin Summary

| Group                    | No. of Pins |
|--------------------------|-------------|
| SDRAM                    | 71          |
| External Peripheral      | 97          |
| External Master          | 9           |
| Internal Peripheral      | 15          |
| Interrupts               | 7           |
| JTAG                     | 5           |
| System                   | 18          |
| <b>Total Signal Pins</b> | <b>222</b>  |
| AV <sub>DD</sub>         | 1           |
| OV <sub>DD</sub>         | 16          |
| V <sub>DD</sub>          | 16          |
| Gnd                      | 40          |
| Thermal (and Gnd)        | 16          |
| Reserved                 | 5           |
| <b>Total Pins</b>        | <b>316</b>  |

### Multiplexed Pins

In the table “Signal Functional Description” on page 23, each I/O signal is listed along with a short description of the signal function. Some signals are multiplexed onto the same package pin (ball) so that the pin can be used for different functions. Multiplexed signals are shown as a default signal with a secondary signal in square brackets (for example, GPIO1[TS1E]). Active-low signals (for example, RAS) are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, the EBC peripheral controller address pins are used as outputs by the PPC405CR to broadcast an address to external slave devices when the PPC405CR has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC405CR.

### Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 39). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

### Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3k $\Omega$  to +3.3V (10k $\Omega$  to +5V can be used on 5V tolerant I/Os) and pull-down value of 1k $\Omega$  to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the PPC405CR.

### Unused I/Os

Strapping of some pins may be necessary when they are unused. Although the PPC405CR requires only the pull-up and pull-down terminations as specified in the “Signal Functional Description” on page 23, good design practice is to terminate all unused inputs or to configure I/Os such that they always drive. If unused, the peripheral and SDRAM buses should be configured and terminated as follows:

- Peripheral interface—PerAddr0:31, PerData0:31, and all of the control signals are driven by default. Terminate PerReady high and PerError low.
- SDRAM—Program SDRAM0\_CFG[EMDULR]=1 and SDRAM0\_CFG[DCE]=1. This causes the PPC405CR to actively drive all of the SDRAM address, data, and control signals.

### External Bus Control Signals

All peripheral bus control signals ( $\overline{\text{PerCS0:7}}$ ,  $\overline{\text{PerR/W}}$ ,  $\overline{\text{PerWBE0:3}}$ ,  $\overline{\text{PerOE}}$ ,  $\overline{\text{PerWE}}$ ,  $\overline{\text{PerBLast}}$ , HoldAck,  $\overline{\text{ExtAck}}$ ) are set to the high-impedance state when  $\overline{\text{ExtReset}}=0$ . In addition, as detailed in the *PowerPC 405CR Embedded Processor User's Manual*, the peripheral bus controller can be programmed via EBC0\_CFG to float some of these control signals between transactions and/or when an external master owns the peripheral bus. As a result, a pull-up resistor should be added to those control signals where an undriven state may affect any devices receiving that particular signal.

The following table lists all of the I/O signals provided by the PPC405CR. Please refer to “Signals Listed Alphabetically” on page 11 for the pin number to which each signal is assigned.

Table 6. Signal Functional Description (Sheet 1 of 5)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

**Notes:**

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull-up or pull-down required.
7. Pull-up may be required. See “External Bus Control Signals” on page 22.

| Signal Name                                | Description   | I/O | Type                       | Notes |
|--|---|-----|----------------------------|-------|
| <b>SDRAM Interface</b>                     |   |     |                            |       |
| MemData0:31                                | Memory Data bus.<br><b>Notes:</b><br>1. MemData0 is the most significant bit (msb).<br>2. MemData31 is the least significant bit (lsb).   | I/O | 3.3V LVTTTL                |       |
| MemAddr12:0                                | Memory Address bus.<br><b>Notes:</b><br>1. MemAddr12 is the most significant bit (msb).<br>2. MemAddr0 is the least significant bit (lsb).  | O   | 3.3V LVTTTL                |       |
| BA0:1                                      | Bank Address supporting up to four internal banks.  | O   | 3.3V LVTTTL                |       |
| $\overline{\text{RAS}}$                    | Row Address Strobe.   | O   | 3.3V LVTTTL                |       |
| $\overline{\text{CAS}}$                    | Column Address Strobe.  | O   | 3.3V LVTTTL                |       |
| DQM0:3                                     | DQM for byte lanes 0 (MemData0:7),<br>1 (MemData8:15),<br>2 (MemData16:23), and<br>3 (MemData24:31).  | O   | 3.3V LVTTTL                |       |
| DQMCB                                      | DQM for ECC check bits.   | O   | 3.3V LVTTTL                |       |
| ECC0:7                                     | ECC check bits 0:7.   | I/O | 3.3V LVTTTL                |       |
| $\overline{\text{BankSel}}0:3$             | Select up to four external SDRAM banks.   | O   | 3.3V LVTTTL                |       |
| $\overline{\text{WE}}$                     | Write Enable.   | O   | 3.3V LVTTTL                |       |
| ClkEn0:1                                   | SDRAM Clock Enable.   | O   | 3.3V LVTTTL                |       |
| MemClkOut0:1                               | Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.  | O   | 3.3V LVTTTL                |       |
| <b>External Slave Peripheral Interface</b> |   |     |                            |       |
| PerData0:31                                | Peripheral data bus used by PPC405CR when not in external master mode, otherwise used by external master.<br><b>Note:</b> PerData0 is the most significant bit (msb) on this bus.   | I/O | 5V tolerant<br>3.3V LVTTTL | 1     |
| PerAddr0:31                                | Peripheral address bus used by PPC405CR when not in external master mode, otherwise used by external master.<br><b>Note:</b> PerAddr0 is the most significant bit (msb) on this bus.  | I/O | 5V tolerant<br>3.3V LVTTTL | 1     |
| PerPar0:3                                  | Peripheral byte parity signals.   | I/O | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{PerWBE}}0:3$              | As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or the DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface. | I/O | 5V tolerant<br>3.3V LVTTTL | 1, 7  |
| $\overline{\text{PerWE}}$                  | Peripheral write enable. Active when any of the four $\overline{\text{PerWBE}}0:3$ signals are active.  | O   | 5V tolerant<br>3.3V LVTTTL |       |

Table 6. Signal Functional Description (Sheet 2 of 5)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

**Notes:**

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull-up or pull-down required.
7. Pull-up may be required. See “External Bus Control Signals” on page 22.

| Signal Name                              | Description   | I/O    | Type                       | Notes |
|--|---|--------|----------------------------|-------|
| $\overline{\text{PerCS0}}$               | Peripheral chip select bank 0.  | O      | 5V tolerant<br>3.3V LVTTTL | 7     |
| $\overline{\text{PerCS1:7}}$ [GPIO10:16] | Seven additional peripheral chip selects<br>or<br>General Purpose I/O. To access this function, software must toggle a DCR register bit.  | O[I/O] | 5V tolerant<br>3.3V LVTTTL | 1, 7  |
| $\overline{\text{PerOE}}$                | Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC405CR is the bus master, it enables the selected device to drive the bus.  | O      | 5V tolerant<br>3.3V LVTTTL | 7     |
| $\overline{\text{PerR/W}}$               | Used by the PPC405CR when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory.<br>Otherwise it used by the external master as an input to indicate the direction of transfer. | I/O    | 5V tolerant<br>3.3V LVTTTL | 1     |
| PerReady                                 | Used by a peripheral slave to indicate it is ready to transfer data.  | I      | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{PerBLast}}$             | Used by the PPC405CR when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.   | I/O    | 5V tolerant<br>3.3V LVTTTL | 1, 7  |
| DMAReq0:3                                | DMAReq0:3 are used by slave peripherals to indicate they are prepared to transfer data.   | I      | 5V tolerant<br>3.3V LVTTTL | 1     |
| DMAAck0:3                                | DMAAck0:3 are used by the PPC405CR to indicate that data transfers have occurred.   | O      | 5V tolerant<br>3.3V LVTTTL | 6     |
| EOT0:3/TC0:3                             | End Of Transfer/Terminal Count.   | I/O    | 5V tolerant<br>3.3V LVTTTL | 1     |



Table 6. Signal Functional Description (Sheet 3 of 5)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

**Notes:**

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull-up or pull-down required.
7. Pull-up may be required. See “External Bus Control Signals” on page 22.

| Signal Name                                 | Description   | I/O | Type                       | Notes |
|---|---|-----|----------------------------|-------|
| <b>External Master Peripheral Interface</b> |   |     |                            |       |
| PerCk                                       | Peripheral clock to be used by an external master and by synchronous peripheral slaves.   | O   | 5V tolerant<br>3.3V LVTTTL |       |
| $\overline{\text{ExtReset}}$                | Peripheral reset to be used by an external master and by synchronous peripheral slaves.   | O   | 5V tolerant<br>3.3V LVTTTL |       |
| HoldReq                                     | Hold Request, used by an external master to request ownership of the peripheral bus.  | I   | 5V tolerant<br>3.3V LVTTTL | 1, 5  |
| HoldAck                                     | Hold Acknowledge, used by the PPC405CR to transfer ownership of peripheral bus to an external master.   | O   | 5V tolerant<br>3.3V LVTTTL | 6     |
| $\overline{\text{ExtReq}}$                  | $\overline{\text{ExtReq}}$ is used by an external master to indicate it is prepared to transfer data.   | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{ExtAck}}$                  | $\overline{\text{ExtAck}}$ is used by the PPC405CR to indicate a data transfer cycle.   | O   | 5V tolerant<br>3.3V LVTTTL | 6     |
| HoldPri                                     | Used by an external master to indicate the priority of a given external master tenure.  | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| BusReq                                      | Used when the PPC405CR needs to regain control of the peripheral interface from an external master.   | O   | 5V tolerant<br>3.3V LVTTTL |       |
| PerErr                                      | Used as an input to indicate that an external slave peripheral error has occurred.  | I   | 5V tolerant<br>3.3V LVTTTL | 1, 5  |
| <b>Internal Peripheral Interface</b>        |   |     |                            |       |
| UARTSerCk                                   | Serial clock. Used to provide an alternate clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either UART. | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| UART0_Rx                                    | UART0 Receive (serial data in).   | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| UART0_Tx                                    | UART0 Transmit (serial data out).   | O   | 5V tolerant<br>3.3V LVTTTL | 6     |
| $\overline{\text{UART0\_DCD}}$              | UART0 Data Carrier Detect.  | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{UART0\_DSR}}$              | UART0 Data Set Ready.   | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{UART0\_CTS}}$              | UART0 Clear To Send.  | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{UART0\_DTR}}$              | UART0 Data Terminal Ready.  | O   | 5V tolerant<br>3.3V LVTTTL | 6     |
| $\overline{\text{UART0\_RTS}}$              | UART0 Request To Send.  | O   | 5V tolerant<br>3.3V LVTTTL | 6     |
| $\overline{\text{UART0\_RI}}$               | UART0 Ring Indicator.   | I   | 5V tolerant<br>3.3V LVTTTL | 1     |
| UART1_Rx                                    | UART1 Receive (serial data in).   | I   | 5V tolerant<br>3.3V LVTTTL | 1     |

Table 6. Signal Functional Description (Sheet 4 of 5)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

**Notes:**

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull-up or pull-down required.
7. Pull-up may be required. See “External Bus Control Signals” on page 22.

| Signal Name                                   | Description  | I/O     | Type                       | Notes |
|---|--|---------|----------------------------|-------|
| UART1_Tx                                      | UART1 Transmit (serial data out).  | O       | 5V tolerant<br>3.3V LVTTTL | 6     |
| $\overline{\text{UART1\_DSR}}$<br>[UART1_CTS] | UART1 Data Set Ready<br>or<br>UART1 Clear To Send. To access this function, software must toggle a DCR register bit.   | I       | 5V tolerant<br>3.3V LVTTTL | 1     |
| $\overline{\text{UART1\_RTS}}$<br>[UART1_DTR] | UART1 Request To Send<br>or<br>UART1 Data Terminal Ready. To access this function, software must toggle a DCR register bit.  | O       | 5V tolerant<br>3.3V LVTTTL | 6     |
| IIC_SCL                                       | IIC serial clock.  | I/O     | 5V tolerant<br>3.3V LVTTTL | 1, 2  |
| IIC_SDA                                       | IIC serial data.   | I/O     | 5V tolerant<br>3.3V LVTTTL | 1, 2  |
| <b>Interrupts Interface</b>                   |  |         |                            |       |
| IRQ0:6[GPIO17:23]                             | Interrupt requests<br>or<br>General Purpose I/O. To access this function, software must toggle a DCR register bit.   | I/[I/O] | 5V tolerant<br>3.3V LVTTTL | 1     |
| <b>JTAG Interface</b>                         |  |         |                            |       |
| TDI   | Test data in.  | I       | 5V tolerant<br>3.3V LVTTTL | 1, 4  |
| TMS   | JTAG test mode select.   | I       | 5V tolerant<br>3.3V LVTTTL | 1, 4  |
| TDO   | Test data out.   | O       | 5V tolerant<br>3.3V LVTTTL |       |
| TCK   | JTAG test clock. The frequency of this input can range from DC to 25MHz.   | I       | 5V tolerant<br>3.3V LVTTTL | 1, 4  |
| $\overline{\text{TRST}}$                      | JTAG reset. $\overline{\text{TRST}}$ must be low at power-on to initialize the JTAG controller and for normal operation of the PPC405CR.   | I       | 5V tolerant<br>3.3V LVTTTL | 5     |
| <b>System Interface</b>                       |  |         |                            |       |
| SysClk  | Main system clock input.   | I       | 5V tolerant<br>3.3V LVTTTL |       |
| $\overline{\text{SysReset}}$                  | Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. Implemented as an open-drain output (two states, 0 or open circuit). | I/O     | 5V tolerant<br>3.3V LVTTTL | 1, 2  |
| SysErr  | Set to 1 when a Machine Check is generated.  | O       | 5V tolerant<br>3.3V LVTTTL |       |
| $\overline{\text{Halt}}$                      | Halt from external debugger.   | I       | 5V tolerant<br>3.3V LVTTTL | 1, 2  |

Table 6. Signal Functional Description (Sheet 5 of 5)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

**Notes:**

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 21 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull-up or pull-down required.
7. Pull-up may be required. See “External Bus Control Signals” on page 22.

| Signal Name                | Description  | I/O    | Type                       | Notes |
|----------------------------|--|--------|----------------------------|-------|
| GPIO1[TS1E]<br>GPIO2[TS2E] | General Purpose I/O<br>or<br>Even Trace execution status. To access this function, software must toggle a DCR register bit.  | I/O[O] | 5V tolerant<br>3.3V LVTTTL | 1, 6  |
| GPIO3[TS1O]<br>GPIO4[TS2O] | General Purpose I/O<br>or<br>Odd Trace execution status. To access this function, software must toggle a DCR register bit.   | I/O[O] | 5V tolerant<br>3.3V LVTTTL | 1, 6  |
| GPIO5:8[TS3:6]             | General Purpose I/O<br><br>Trace status. To access this function, software must toggle a DCR register bit.   | I/O[O] | 5V tolerant<br>3.3V LVTTTL | 1     |
| GPIO9[TrcClk]              | General Purpose I/O<br>or<br>Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR register bit. | I/O[O] | 5V tolerant<br>3.3V LVTTTL | 1     |
| TestEn                     | Test Enable.   | I      | 2.5V CMOS<br>w/pull-down   |       |
| RcvrInh                    | Receiver Inhibit. Used only for manufacturing tests. Pull up for normal operation.   | I      | 5V tolerant<br>3.3V LVTTTL | 2     |
| DrvrInh1:2                 | Driver Inhibit 1 and 2. Used only for manufacturing tests. Pull up for normal operation.   | I      | 5V tolerant<br>3.3V LVTTTL | 2     |
| TmrClk                     | An external clock input than can be used as an alternative to SysClk to run the CPU core. Which clock input is used is determined by software settings.                                | I      | 5V tolerant<br>3.3V LVTTTL | 1     |
| <b>Power</b>               |  |        |                            |       |
| GND                        | Ground<br><b>Note:</b> Pins J9–J12, K9–K12, L9–L12, and M9–M12 are also thermal balls.   |        |                            |       |
| AV <sub>DD</sub>           | Filtered voltage input for PLL (analog) circuits   |        |                            |       |
| OV <sub>DD</sub>           | Output driver voltage—3.3V   |        |                            |       |
| V <sub>DD</sub>            | Logic voltage—2.5V   |        |                            |       |
| <b>Other pins</b>          |  |        |                            |       |
| Reserved                   | Connect G19 to GND. Do not connect signals, voltage, or ground to any other reserved pins.   |        |                            |       |

**Table 7. Absolute Maximum Ratings**

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

| Characteristic                        | Symbol    | Value                 | Unit |
|---------------------------------------|-----------|-----------------------|------|
| Supply Voltage (Internal Logic)       | $V_{DD}$  | 0 to +2.7             | V    |
| Supply Voltage (I/O Interface)        | $OV_{DD}$ | 0 to +3.6             | V    |
| PLL Supply Voltage                    | $AV_{DD}$ | 0 to +2.7             | V    |
| Input Voltage (2.5V CMOS receivers)   | $V_{IN}$  | -0.6 to $V_{DD}+0.6$  | V    |
| Input Voltage (3.3V LVTTTL receivers) | $V_{IN}$  | -0.6 to $OV_{DD}+0.6$ | V    |
| Input Voltage (5.0V LVTTTL receivers) | $V_{IN}$  | -0.6 to $OV_{DD}+2.4$ | V    |
| Storage Temperature Range             | $T_{STG}$ | -55 to +150           | °C   |
| Case temperature under bias           | $T_C$     | -40 to +120           | °C   |

**Note:** All specified voltages are with respect to GND.

**Figure 3. Package Thermal Specifications**

The PPC405CR is designed to operate within a case temperature range of -40°C to +85°C. Thermal resistance values for the E-PBGA package in a convection environment are as follows:

| Thermal Resistance           | Symbol        | Airflow<br>ft/min (m/sec) |            |            | Unit |
|------------------------------|---------------|---------------------------|------------|------------|------|
|                              |               | 0 (0)                     | 100 (0.51) | 200 (1.02) |      |
| Junction-to-case             | $\theta_{JC}$ | 2                         | 2          | 2          | °C/W |
| Case-to-ambient <sup>1</sup> | $\theta_{CA}$ | 18                        | 16         | 15         | °C/W |

**Notes:**

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
  - a. Case temperature,  $T_C$ , is measured at top center of case surface with device soldered to circuit board.
  - b.  $T_A = T_C - P \times \theta_{CA}$ , where  $T_A$  is ambient temperature and P is power consumption.
  - c.  $T_{CMax} = T_{JMax} - P \times \theta_{JC}$ , where  $T_{JMax}$  is maximum junction temperature and P is power consumption.

Table 8. Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

| Parameter   | Symbol       | Minimum         | Typical | Maximum            | Unit        | Notes |
|---|--------------|-----------------|---------|--------------------|-------------|-------|
| Logic Supply Voltage                                    | $V_{DD}$     | +2.3            | +2.5    | +2.7               | V           |       |
| I/O Supply Voltage                                      | $OV_{DD}$    | +3.0            | +3.3    | +3.6               | V           |       |
| PLL Supply Voltage                                      | $AV_{DD}$    | +2.3            | +2.5    | +2.7               | V           |       |
| Input Logic High<br>(2.5V CMOS receivers)               | $V_{IH}$     | +1.7            |         | $V_{DD}$           | V           |       |
| Input Logic High<br>(3.3V LVTTL receivers)              | $V_{IH}$     | +2.0            |         | $OV_{DD}$          | V           |       |
| Input Logic High<br>(5.0V LVTTL receivers)              | $V_{IH}$     | +2.0            |         | +5.0               | V           |       |
| Input Logic Low<br>(2.5V CMOS receivers)                | $V_{IL}$     | 0               |         | +0.7               | V           |       |
| Input Logic Low<br>(3.3/5.0V LVTTL receivers)           | $V_{IL}$     | 0               |         | +0.8               | V           |       |
| Output Logic High                                       | $V_{OH}$     | +2.4            |         | $OV_{DD}$          | V           |       |
| Output Logic Low  | $V_{OL}$     | 0               |         | +0.4               | V           |       |
| 3.3V I/O Input Current (no pull-up or pull-down)        | $I_{IL1}$    |                 |         | $\pm 10$           | $\mu A$     |       |
| Input Current (with internal pull-down)                 | $I_{IL2}$    | $\pm 10$ (@ 0V) |         | +400 (@ $V_{DD}$ ) | $\mu A$     |       |
| 5V Tolerant I/O Input Current <sup>1</sup>              | $I_{IL4}$    | $\pm 10$        |         | -650               | $\mu A$     |       |
| Input Max Allowable Overshoot<br>(2.5V CMOS receivers)  | $V_{IMAO25}$ |                 |         | $V_{DD} + 0.6$     | V           |       |
| Input Max Allowable Overshoot<br>(3.3V LVTTL receivers) | $V_{IMAO3}$  |                 |         | $OV_{DD} + 0.6$    | V           |       |
| Input Max Allowable Overshoot<br>(5.0V LVTTL receivers) | $V_{IMAO5}$  |                 |         | +5.5               | V           |       |
| Input Max Allowable Undershoot                          | $V_{IMAU}$   | -0.6            |         |                    | V           |       |
| Output Max Allowable Overshoot                          | $V_{OMAO}$   |                 |         | $OV_{DD} + 0.3$    | V           |       |
| Output Max Allowable Undershoot                         | $V_{OMAU3}$  | -0.6            |         |                    | V           |       |
| Case Temperature  | $T_C$        | -40             |         | +85                | $^{\circ}C$ |       |

**Notes:**

1. See "5V-Tolerant I/O Input Current" on page 30

Figure 4. 5V-Tolerant I/O Input Current

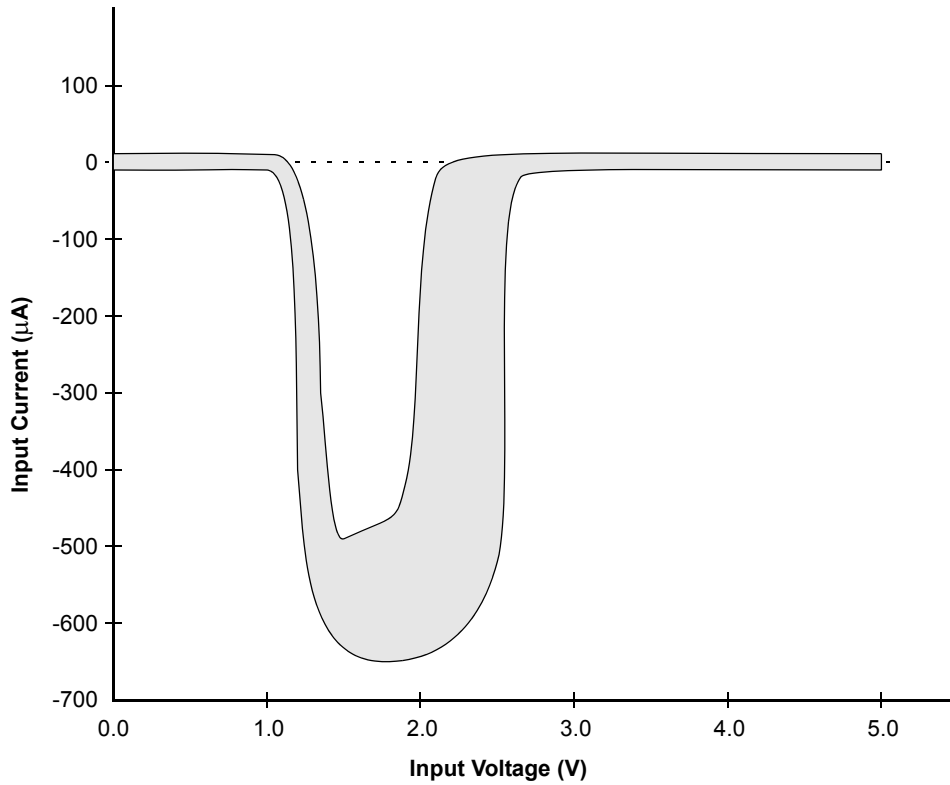


Table 9. Input Capacitance

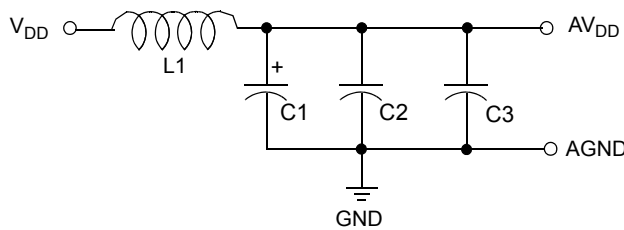
| Parameter              | Symbol           | Maximum | Unit | Notes |
|------------------------|------------------|---------|------|-------|
| 3.3V LVTTTL I/O        | C <sub>IN1</sub> | 5.4     | pF   |       |
| 5V tolerant LVTTTL I/O | C <sub>IN2</sub> | 4.4     | pF   |       |
| RX only pins           | C <sub>IN4</sub> | 3.4     | pF   |       |

Table 10. DC Electrical Characteristics

| Parameter                                     | Symbol    | Minimum | Typical | Maximum | Unit |
|---|-----------|---------|---------|---------|------|
| Active Operating Current ( $V_{DD}$ )—133MHz  | $I_{DD}$  |         | TBD     | TBD     | mA   |
| Active Operating Current ( $OV_{DD}$ )—133MHz | $I_{ODD}$ |         | TBD     | TBD     | mA   |
| Active Operating Current ( $V_{DD}$ )—200MHz  | $I_{DD}$  |         | 400     | 610     | mA   |
| Active Operating Current ( $OV_{DD}$ )—200MHz | $I_{ODD}$ |         | 35      | 40      | mA   |
| Active Operating Current ( $V_{DD}$ )—266MHz  | $I_{DD}$  |         | TBD     | TBD     | mA   |
| Active Operating Current ( $OV_{DD}$ )—266MHz | $I_{ODD}$ |         | TBD     | TBD     | mA   |
| PLL $V_{DD}$ Input current                    | $I_{PLL}$ |         | 16      | 23      | mA   |

**Note:**

- Maximum power is characterized at  $V_{DD} = 2.7V$ ,  $OV_{DD} = 3.6V$ ,  $T_C = 85^\circ C$ , across the silicon process (worse case to best case), while running an application designed to maximize power consumption. The specification at 200MHz corresponds to CPU = 200 MHz, PLB = 100MHz, OPB = EBC = 50MHz. The 266MHz maximum power was measured with CPU = 266.6MHz, PLB =133.3MHz, OPB = EBC = 66.6MHz.
- $AV_{DD}$  should be derived from  $V_{DD}$  using the following circuit:



- L1 – 2.2 $\mu$ H SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700S)
- C1 – 3.3  $\mu$ F SMT tantalum
- C2 – 0.1  $\mu$ F SMT monolithic ceramic capacitor with X7R dielectric or equivalent
- C3 – 0.01  $\mu$ F SMT monolithic ceramic capacitor with X7R dielectric or equivalent

**Test Conditions**

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at  $OV_{DD} = 3V$  and  $T_J = +85^\circ C$  with the 50pF test load shown in the figure at right.

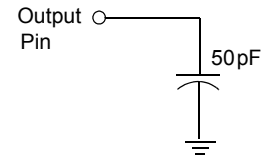
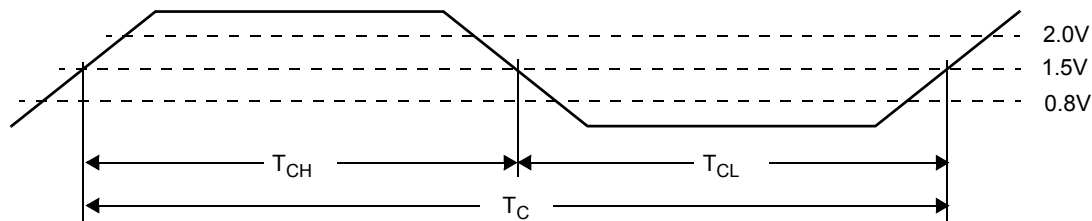


Table 11. Clocking Specifications

| Symbol                               | Parameter   | Min                   | Max                   | Units |
|--------------------------------------|---|-----------------------|-----------------------|-------|
| <b>CPU</b>                           |   |                       |                       |       |
| PF <sub>C</sub>                      | Processor clock frequency                           | 133.33/200/266.66     |                       | MHz   |
| PT <sub>C</sub>                      | Processor clock period                              | 7.5/5/3.75            |                       | ns    |
| <b>SysClk Input</b>                  |   |                       |                       |       |
| SCF <sub>C</sub>                     | Clock input frequency                               | 25                    | 66.66                 | MHz   |
| SCT <sub>C</sub>                     | Clock period  | 15                    | 40                    | ns    |
| SCT <sub>CS</sub>                    | Clock edge stability (phase jitter, cycle to cycle) |                       | ± 0.15                | ns    |
| SCT <sub>CH</sub>                    | Clock input high time                               | 40% of nominal period | 60% of nominal period | ns    |
| SCT <sub>CL</sub>                    | Clock input low time                                | 40% of nominal period | 60% of nominal period | ns    |
| <b>Note:</b> Input slew rate > 2V/ns |   |                       |                       |       |
| <b>MemClkOut Output</b>              |   |                       |                       |       |
| MCOF <sub>C</sub>                    | Clock output frequency @ PF <sub>C</sub> = 133MHz   |                       | 66.66                 | MHz   |
| MCOT <sub>C</sub>                    | Clock period @ PF <sub>C</sub> = 133MHz             | 15                    |                       | ns    |
| MCOF <sub>C</sub>                    | Clock output frequency @ PF <sub>C</sub> = 200MHz   |                       | 100                   | MHz   |
| MCOT <sub>C</sub>                    | Clock period @ PF <sub>C</sub> = 200MHz             | 10                    |                       | ns    |
| MCOF <sub>C</sub>                    | Clock output frequency @ PF <sub>C</sub> = 266MHz   |                       | 133.33                | MHz   |
| MCOT <sub>C</sub>                    | Clock period @ PF <sub>C</sub> = 266MHz             | 7.5                   |                       | ns    |
| MCOT <sub>CS</sub>                   | Clock edge stability (phase jitter, cycle to cycle) |                       | ± 0.2                 | ns    |
| MCOT <sub>CH</sub>                   | Clock output high time                              | 45% of nominal period | 55% of nominal period | ns    |
| MCOT <sub>CL</sub>                   | Clock output low time                               | 45% of nominal period | 55% of nominal period | ns    |
| <b>Other Clocks</b>                  |   |                       |                       |       |
| VCOF <sub>C</sub>                    | VCO frequency                                       | 400                   | 800                   | MHz   |
| PLBF <sub>C</sub>                    | PLB frequency @ PF <sub>C</sub> = 133MHz            |                       | 66.66                 | MHz   |
| PLBF <sub>C</sub>                    | PLB frequency @ PF <sub>C</sub> = 200MHz            |                       | 100                   | MHz   |
| PLBF <sub>C</sub>                    | PLB frequency @ PF <sub>C</sub> = 266MHz            |                       | 133.33                | MHz   |
| OPBF <sub>C</sub>                    | OPB frequency @ PF <sub>C</sub> = 133MHz            |                       | 33.33                 | MHz   |
| OPBF <sub>C</sub>                    | OPB frequency @ PF <sub>C</sub> = 200MHz            |                       | 50                    | MHz   |
| OPBF <sub>C</sub>                    | OPB frequency @ PF <sub>C</sub> = 266MHz            |                       | 66.66                 | MHz   |

Figure 5. Timing Waveform





## Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC405CR. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC405CR the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405CR with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board PPC405CR peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock (PerClk) for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClkOut since it also tracks the modulation.

### Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation.
2. IIC operation is unaffected.

**Caution:** It is up to the system designer to ensure that any SSCG used with the PPC405CR meets the above requirements and does not adversely affect other aspects of the system.

Table 12. Peripheral Interface Clock Timings

| Parameter  | Min                   | Max                           | Units |
|--|-----------------------|-------------------------------|-------|
| PerClk output frequency—133MHz                             | –                     | 33.33                         | MHz   |
| PerClk period—133MHz                                       | 30                    | –                             | ns    |
| PerClk output frequency—200MHz                             | –                     | 50                            | MHz   |
| PerClk period—200MHz                                       | 20                    | –                             | ns    |
| PerClk output frequency—266MHz                             | –                     | 66.66                         | MHz   |
| PerClk period—266MHz                                       | 15                    | –                             | ns    |
| PerClk output high time                                    | 45% of nominal period | 55% of nominal period         | ns    |
| PerClk output low time                                     | 45% of nominal period | 55% of nominal period         | ns    |
| PerClk clock edge stability (phase jitter, cycle to cycle) |                       | ± 0.3                         | ns    |
| UARTSerClk input frequency (Note 1)                        | –                     | 1000/(2T <sub>OPB</sub> +2ns) | MHz   |
| UARTSerClk period  | 2T <sub>OPB</sub> +2  | –                             | ns    |
| UARTSerClk input high time                                 | T <sub>OPB</sub> +1   | –                             | ns    |
| UARTSerClk input low time                                  | T <sub>OPB</sub> +1   | –                             | ns    |
| TmrClk input frequency—133MHz                              | –                     | 33.33                         | MHz   |
| TmrClk period—133MHz                                       | 30                    | –                             | ns    |
| TmrClk input frequency—200MHz                              | –                     | 50                            | MHz   |
| TmrClk period—200MHz                                       | 20                    | –                             | ns    |
| TmrClk input frequency—266MHz                              | –                     | 66.66                         | MHz   |
| TmrClk period—266MHz                                       | 15                    | –                             | ns    |
| TmrClk input high time                                     | 40% of nominal period | 60% of nominal period         | ns    |
| TmrClk input low time                                      | 40% of nominal period | 60% of nominal period         | ns    |

**Notes:**

1. T<sub>OPB</sub> is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 50MHz for 200MHz parts and 66.66MHz for 266MHz parts.

Figure 6. Input Setup and Hold Waveform

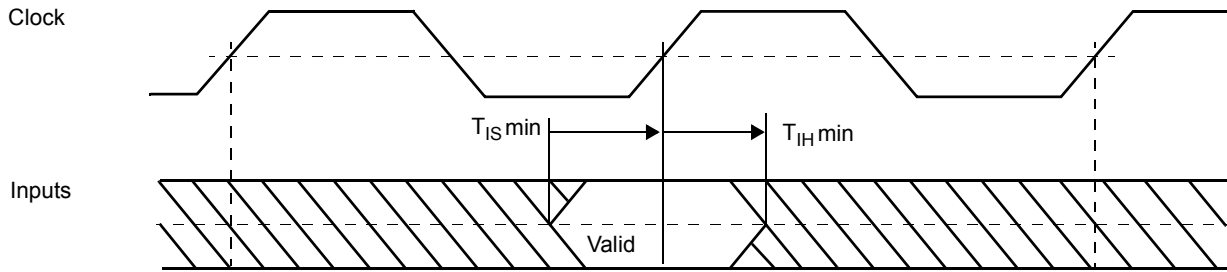
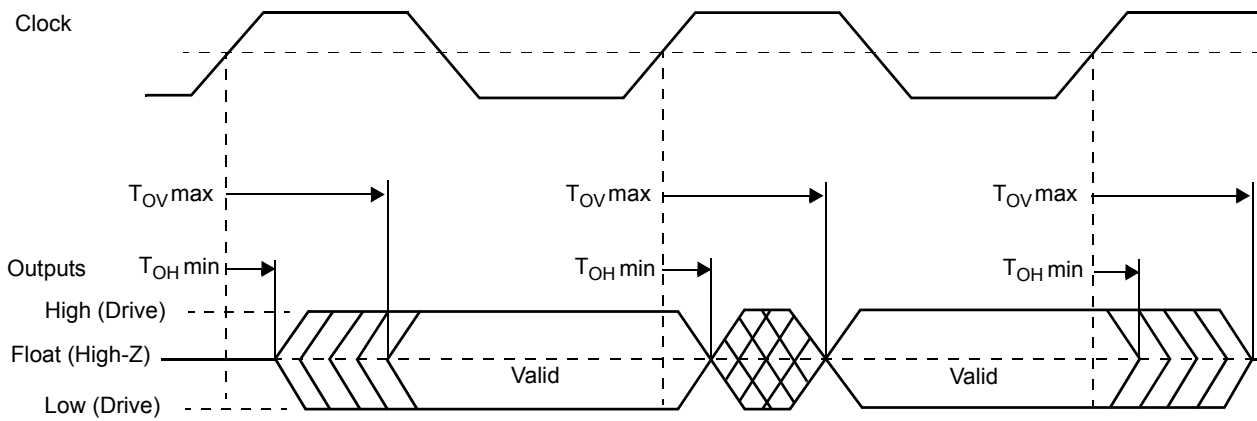


Figure 7. Output Delay and Float Timing Waveform



- Notes:** 1. In all of the following I/O Specifications tables a timing value of na means “not applicable” and dc means “don’t care.”  
 2. See “Test Conditions” on page 31 for output capacitive loading.  
 3. I/O H is specified at 2.4V; I/O L is specified at 0.4V

Table 13. I/O Specifications—All speeds

| Signal  | Input (ns)                       |                                 | Output (ns)                       |                                 | Output Current (mA) |             | Clock | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-------------|-------|-------|
|   | Setup Time (T <sub>IS</sub> min) | Hold Time (T <sub>IH</sub> min) | Valid Delay (T <sub>OV</sub> max) | Hold Time (T <sub>OH</sub> min) | I/O H (min)         | I/O L (min) |       |       |
| <b>Internal Peripheral Interface</b>  |                                  |                                 |                                   |                                 |                     |             |       |       |
| IIC_SCL   | n/a                              | n/a                             | n/a                               | n/a                             | 19                  | 12          |       |       |
| IIC_SDA   | n/a                              | n/a                             | n/a                               | n/a                             | 19                  | 12          |       |       |
| UART0_CTS   | n/a                              | n/a                             |                                   |                                 | 12                  | 8           |       |       |
| UART0_DCD   | n/a                              | n/a                             |                                   |                                 | 12                  | 8           |       |       |
| UART0_DSR   | n/a                              | n/a                             |                                   |                                 | 12                  | 8           |       |       |
| UART0_DTR   |                                  |                                 |                                   |                                 | 12                  | 8           |       |       |
| UART0_RI  | n/a                              | n/a                             |                                   |                                 | 12                  | 8           |       |       |
| UART0_RTS   |                                  |                                 | n/a                               | n/a                             | 12                  | 8           |       |       |
| UART0_Rx  | n/a                              | n/a                             |                                   |                                 | 12                  | 8           |       |       |
| UART0_Tx  |                                  |                                 | n/a                               | n/a                             | 12                  | 8           |       |       |
| UART1_RTS<br>[UART1_DTR]  |                                  |                                 | n/a                               | n/a                             | 12                  | 8           |       |       |
| UART1_DSR<br>[UART1_CTS]  | n/a                              | n/a                             |                                   |                                 | n/a                 | n/a         |       |       |
| UART1_Rx  | n/a                              | n/a                             |                                   |                                 | n/a                 | n/a         |       |       |
| UART1_Tx  |                                  |                                 | n/a                               | n/a                             | 12                  | 8           |       |       |
| UARTSerClk  | n/a                              | n/a                             |                                   |                                 | n/a                 | n/a         |       |       |
| <b>Interrupts Interface</b>   |                                  |                                 |                                   |                                 |                     |             |       |       |
| IRQ0:6[GPIO17:23]   |                                  |                                 |                                   |                                 | 12                  | 8           |       |       |
| <b>JTAG Interface</b>   |                                  |                                 |                                   |                                 |                     |             |       |       |
| TCK   |                                  |                                 |                                   |                                 | n/a                 | n/a         |       | async |
| TDI   |                                  |                                 |                                   |                                 | n/a                 | n/a         |       | async |
| TDO   |                                  |                                 |                                   |                                 | 12                  | 8           |       | async |
| TMS   |                                  |                                 |                                   |                                 | n/a                 | n/a         |       | async |
| TRST  |                                  |                                 |                                   |                                 | n/a                 | n/a         |       | async |
| <b>System Interface</b>   |                                  |                                 |                                   |                                 |                     |             |       |       |
| Drvrlnh1:2  | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         |       |       |
| GPIO1[TS1E]<br>GPIO2[TS2E]<br>GPIO3[TS1O]<br>GPIO4[TS2O]<br>GPIO5[TS3]<br>GPIO6[TS4]<br>GPIO7[TS5]<br>GPIO8[TS6]<br>GPIO9[TrcClk] |                                  |                                 |                                   |                                 | 12                  | 8           |       |       |
| Halt  | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         |       | async |
| Rcvrlnh   | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         |       |       |
| SysClk  |                                  |                                 | n/a                               | n/a                             | n/a                 | n/a         |       |       |
| SysErr  |                                  |                                 | n/a                               | n/a                             | 12                  | 8           |       | async |
| SysReset  |                                  |                                 | 10                                | 1                               | 12                  | 8           |       | async |
| TestEn  | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         |       | async |
| TmrClk  | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         |       | async |

Table 14. I/O Specifications—133 and 200MHz

**Notes:**

1. The SDRAM command interface is configurable through SDRAM0\_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM.
2. SDRAM I/O timings are specified relative to a MemClkOut terminated into a lumped 10pF load.
3. SDRAM interface hold times are guaranteed at the PPC405CR package pin. System designers must use the PPC405CR IBIS model (available from [www.amcc.com](http://www.amcc.com)) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
5. I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

| Signal                                      | Input (ns)                       |                                 | Output (ns)                       |                                 | Output Current (mA) |             | Clock     | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-------------|-----------|-------|
|   | Setup Time (T <sub>IS</sub> min) | Hold Time (T <sub>IH</sub> min) | Valid Delay (T <sub>OV</sub> max) | Hold Time (T <sub>OH</sub> min) | I/O H (min)         | I/O L (min) |           |       |
| <b>SDRAM Interface</b>                      |                                  |                                 |                                   |                                 |                     |             |           |       |
| BA1:0                                       | n/a                              | n/a                             | 7.3                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| BankSel0:3                                  | n/a                              | n/a                             | 5.8                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| CAS   | n/a                              | n/a                             | 7.3                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| ClkEn0:1                                    | n/a                              | n/a                             | 4.7                               | 1                               | 40                  | 25          | MemClkOut | 2     |
| DQM0:3                                      | n/a                              | n/a                             | 6.2                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| DQMCB                                       | n/a                              | n/a                             | 6                                 | 1                               | 19                  | 12          | MemClkOut | 2     |
| ECC0:7                                      | 2                                | 1                               | 6                                 | 1                               | 19                  | 12          | MemClkOut | 2     |
| MemAddr12:0                                 | n/a                              | n/a                             | 7.8                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| MemData0:31                                 | 2                                | 1                               | 6.2                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| RAS   | n/a                              | n/a                             | 7.4                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| WE  | n/a                              | n/a                             | 7.4                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| <b>External Slave Peripheral Interface</b>  |                                  |                                 |                                   |                                 |                     |             |           |       |
| DMAAck0:3                                   | n/a                              | n/a                             | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| DMAReq0:3                                   | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| EOT0:3/TC0:3                                | dc                               | dc                              | 9                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerAddr0:31                                 | 4                                | 1                               | 10                                | 0                               | 19                  | 12          | PerClk    |       |
| PerBLast                                    | 4                                | 1                               | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerCS0<br>PerCS1:7[GPIO10:16]               | n/a                              | n/a                             | 9                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerData0:31                                 | 6                                | 1                               | 10                                | 0                               | 19                  | 12          | PerClk    |       |
| PerOE                                       | n/a                              | n/a                             | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerPar0:3                                   | 4                                | 1                               | 10.5                              | 0                               | 19                  | 12          | PerClk    |       |
| PerR/W                                      | 5                                | 1                               | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerReady                                    | 9                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| PerWBE0:3                                   | 4                                | 1                               | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| <b>External Master Peripheral Interface</b> |                                  |                                 |                                   |                                 |                     |             |           |       |
| BusReq                                      | n/a                              | n/a                             | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| ExtAck                                      | n/a                              | n/a                             | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| ExtReq                                      | 6                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| ExtReset                                    | n/a                              | n/a                             | 8                                 | 0                               | 19                  | 12          | PerClk    |       |
| HoldAck                                     | n/a                              | n/a                             | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| HoldPri                                     | 4                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| HoldReq                                     | 6                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| PerClk                                      | n/a                              | n/a                             | 0.9                               | 0.9                             | 19                  | 12          | PLB Clk   | 4     |
| PerErr                                      | 4                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |

Table 15. I/O Specifications—266MHz

**Notes:**

1. The SDRAM command interface is configurable through SDRAM0\_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM.
2. SDRAM I/O timings are specified relative to a MemClkOut terminated into a lumped 10pF load.
3. SDRAM interface hold times are guaranteed at the PPC405CR package pin. System designers must use the PPC405CR IBIS model (available from [www.amcc.com](http://www.amcc.com)) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
5. I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

| Signal                                      | Input (ns)                       |                                 | Output (ns)                       |                                 | Output Current (mA) |             | Clock     | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-------------|-----------|-------|
|   | Setup Time (T <sub>IS</sub> min) | Hold Time (T <sub>IH</sub> min) | Valid Delay (T <sub>Ov</sub> max) | Hold Time (T <sub>OH</sub> min) | I/O H (min)         | I/O L (min) |           |       |
| <b>SDRAM Interface</b>                      |                                  |                                 |                                   |                                 |                     |             |           |       |
| BA1:0                                       | n/a                              | n/a                             | 5.5                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| BankSel0:3                                  | n/a                              | n/a                             | 4.5                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| CAS   | n/a                              | n/a                             | 5.5                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| ClkEn0:1                                    | n/a                              | n/a                             | 3.9                               | 1                               | 40                  | 25          | MemClkOut | 2     |
| DQM0:3                                      | n/a                              | n/a                             | 4.9                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| DQMCB                                       | n/a                              | n/a                             | 4.7                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| ECC0:7                                      | 1.5                              | 1                               | 4.7                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| MemAddr12:0                                 | n/a                              | n/a                             | 5.9                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| MemData0:31                                 | 1.5                              | 1                               | 4.8                               | 1                               | 19                  | 12          | MemClkOut | 2     |
| RAS   | n/a                              | n/a                             | 5.6                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| WE  | n/a                              | n/a                             | 5.6                               | 1                               | 19                  | 12          | MemClkOut | 1, 2  |
| <b>External Slave Peripheral Interface</b>  |                                  |                                 |                                   |                                 |                     |             |           |       |
| DMAAck0:3                                   | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| DMAReq0:3                                   | dc                               | dc                              | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| EOT0:3/TC0:3                                | dc                               | dc                              | 8                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerAddr0:31                                 | 3                                | 1                               | 8                                 | 0                               | 19                  | 12          | PerClk    |       |
| PerBLast                                    | 3.5                              | 1                               | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerCS0<br>PerCS1:7[GPIO10:16]               | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerData0:31                                 | 5                                | 1                               | 8                                 | 0                               | 19                  | 12          | PerClk    |       |
| PerOE                                       | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerPar0:3                                   | 3.5                              | 1                               | 8                                 | 0                               | 19                  | 12          | PerClk    |       |
| PerR/W                                      | 4                                | 1                               | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| PerReady                                    | 6.5                              | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| PerWBE0:3                                   | 3                                | 1                               | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| <b>External Master Peripheral Interface</b> |                                  |                                 |                                   |                                 |                     |             |           |       |
| BusReq                                      | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| ExtAck                                      | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| ExtReq                                      | 5                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| ExtReset                                    | n/a                              | n/a                             | 6                                 | 0                               | 19                  | 12          | PerClk    |       |
| HoldAck                                     | n/a                              | n/a                             | 6                                 | 0                               | 12                  | 8           | PerClk    |       |
| HoldPri                                     | 3                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| HoldReq                                     | 5                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |
| PerClk                                      | n/a                              | n/a                             | 0.9                               | 0.9                             | 19                  | 12          | PLB Clk   | 4     |
| PerErr                                      | 3                                | 1                               | n/a                               | n/a                             | n/a                 | n/a         | PerClk    |       |

**Strapping**

When the SysReset input is driven low by an external device (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405CR start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V or 10kΩ to +5V. The recommended pull-down is 1KΩ to GND. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options. The signal names assigned to the pins for normal operation follow the pin number.

Table 16. Strapping Pin Assignments (Sheet 1 of 2)

| Function  | Option                       | Ball Strapping            |                           |                  |
|---|------------------------------|---------------------------|---------------------------|------------------|
|   |                              | W15<br>UART0_Tx           | U13<br>UART0_DTR          | V20<br>UART0_RTS |
| PLL Tuning <sup>1</sup><br>for $6 \leq M \leq 7$ use choice 3<br>for $7 < M \leq 12$ use choice 5<br>for $12 < M \leq 32$ use choice 6<br>See Note. | Choice 1; TUNE[5:0] = 010001 | 0                         | 0                         | 0                |
|   | Choice 2; TUNE[5:0] = 010010 | 0                         | 0                         | 1                |
|   | Choice 3; TUNE[5:0] = 010011 | 0                         | 1                         | 0                |
|   | Choice 4; TUNE[5:0] = 010100 | 0                         | 1                         | 1                |
|   | Choice 5; TUNE[5:0] = 010101 | 1                         | 0                         | 0                |
|   | Choice 6; TUNE[5:0] = 010110 | 1                         | 0                         | 1                |
|   | Choice 7; TUNE[5:0] = 010111 | 1                         | 1                         | 0                |
|   | Choice 8; TUNE[5:0] = 100100 | 1                         | 1                         | 1                |
| PLL Forward Divider <sup>2</sup>  |                              | <b>C16</b><br>DMAAck0     | <b>B17</b><br>DMAAck1     |                  |
|   | Bypass mode                  | 0                         | 0                         |                  |
|   | Divide by 3                  | 0                         | 1                         |                  |
|   | Divide by 4                  | 1                         | 0                         |                  |
| PLL Feedback Divider <sup>2</sup>   |                              | <b>B16</b><br>DMAAck2     | <b>A14</b><br>DMAAck3     |                  |
|   | Divide by 1                  | 0                         | 0                         |                  |
|   | Divide by 2                  | 0                         | 1                         |                  |
|   | Divide by 3                  | 1                         | 0                         |                  |
| PLB Divider from CPU <sup>2, 3</sup>  |                              | <b>B18</b><br>GPIO1[TS1E] | <b>D16</b><br>GPIO2[TS2E] |                  |
|   | Divide by 1                  | 0                         | 0                         |                  |
|   | Divide by 2                  | 0                         | 1                         |                  |
|   | Divide by 3                  | 1                         | 0                         |                  |
| OPB Divider from PLB <sup>2</sup>   |                              | <b>T4</b><br>HoldAck      | <b>U5</b><br>ExtAck       |                  |
|   | Divide by 1                  | 0                         | 0                         |                  |
|   | Divide by 2                  | 0                         | 1                         |                  |
|   | Divide by 3                  | 1                         | 0                         |                  |
| OPB Divider from PLB <sup>2</sup>   |                              | <b>T4</b><br>HoldAck      | <b>U5</b><br>ExtAck       |                  |
|   | Divide by 1                  | 0                         | 0                         |                  |
|   | Divide by 2                  | 0                         | 1                         |                  |
|   | Divide by 3                  | 1                         | 0                         |                  |
| OPB Divider from PLB <sup>2</sup>   |                              | <b>T4</b><br>HoldAck      | <b>U5</b><br>ExtAck       |                  |
|   | Divide by 1                  | 0                         | 0                         |                  |
|   | Divide by 2                  | 0                         | 1                         |                  |
|   | Divide by 3                  | 1                         | 0                         |                  |

Table 16. Strapping Pin Assignments (Sheet 2 of 2)

| Function                                      | Option      | Ball Strapping            |                                      |
|---|-------------|---------------------------|--------------------------------------|
| External Bus Divider from PLB <sup>2, 3</sup> |             | <b>C17</b><br>GPIO3[TS10] | <b>P18</b><br>GPIO4[TS20]            |
|   | Divide by 2 | 0                         | 0                                    |
|   | Divide by 3 | 0                         | 1                                    |
|   | Divide by 4 | 1                         | 0                                    |
|   | Divide by 5 | 1                         | 1                                    |
| ROM Width                                     |             | <b>Y5</b><br>UART1_Tx     | <b>W6</b><br>UART1_RTS/<br>UART1_DTR |
|   | 8-bit ROM   | 0                         | 0                                    |
|   | 16-bit ROM  | 0                         | 1                                    |
|   | 32-bit ROM  | 1                         | 0                                    |
|   | Reserved    | 1                         | 1                                    |

**Note:**

1. The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the PPC405CR. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the PPC405CR, visit the technical documents area of the AMCC PowerPC web site.
2. Not all combinations of dividers produce valid operating configurations. Frequencies must be within the limits specified in "Clocking Specifications" on page 32. Further requirements are detailed in the Clocking chapter of the *PowerPC 405CR Embedded Processor User's Manual*.
3. Additional consideration must be given to pins that normally function as Trace signals. Improved design margin can be gained by using three-state buffers instead of strapping resistors, and minimizing trace lengths and stubs.



**Document Revision History**

| Revision | Date     | Description                 |
|----------|----------|-----------------------------|
| 1.01     | 08/05/04 | Initial release             |
| 1.02     | 01/11/05 | Add lead-free part numbers. |



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